Designing a BCM® Pre-Charge Circuit

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Introduction

This document provides guidelines on how to design the appropriate pre-charge circuit for applications that require a load capacitance that exceeds the specification of BCM products. The suggested design does not include any components within the main power path and is not impacted by the crippling effects of a high continuous current solution.

Theory

The isolation transformation within a BCM allows the effective output capacitance to be efficiently transferred to the input. The relationship of output capacitance as a function of input capacitance is defined by the Equation 1 below.

It is recommended to use an effective low capacitance at the input of the BCM to minimize the size and number of capacitors used in a typical application.

Some applications require a high load capacitance that cannot be modified. This can be problematic when powering BCMs due to their maximum effective output capacitance (external) specification. If this specification is exceeded the BCM will enter short circuit protection mode due to the high inrush current from charging the capacitors.

A simple solution to this obstruction is to trick the BCM into treating the capacitor charging as a load transient. By allowing the BCM to first reach steady state operation, it will then be ready to process full power. Additionally, by increasing the charging period of the capacitor it lessens the impact of the pulsed current on the BCM. This can be done by using a MOSFET to temporarily disconnect the output capacitor. An additional RC circuit combined with a resistive divider is required to delay the threshold voltage from being reached too quickly. Once the BCM output voltage reaches steady state the MOSFET will turn on and allow a limited current to flow.

$$C_{OUT} = \frac{C_{IN}}{K^2} \qquad (1)$$

N-Channel Power MOSFET

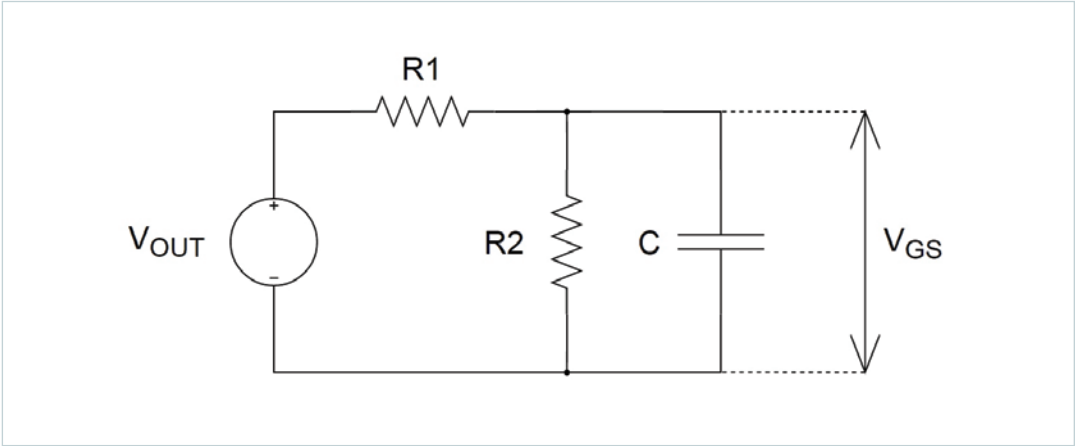
Placing a MOSFET between the output capacitor and –OUT of the BCM prevents any charge current from passing until a threshold voltage is reached. It also acts as a buffer to limit the current surge that causes failures during BCM startup conditions. The drain of the MOSFET should be connected to the negative polarity pin (if there is one) of the load capacitor and the source should be directly connected to –OUT. This configuration allows the gate voltage to be directly referenced to the respective ground when switching on the MOSFET.

When selecting an N-Channel power MOSFET it is desirable to use a drain-to-source voltage, V_{DS}, and a pulsed drain current, I_{DM}, that does not exceed the maximum output voltage or current of the BCM. Another attribute needed is a maximum threshold voltage, $V_{GS(TH)}$, that is less than the output voltage of the BCM. Other characteristics to consider, which are application specific, may include switching speed, ISM and $R_{DS(ON)}$. For this example we will use an IRF510 N-Channel power MOSFET. The chosen MOSFET has a fast switching speed, 100V V_{DS}, less than 1Ω $R_{DS(on)}$, 2V $V_{GS(TH)}$ and a 20A pulsed drain and diode current limit. These specifications are appropriate for supplying a charging current up to 20A for a 12V bus architecture with a relatively quick start up response.

RC Time Constant

The following figure represents a simple RC circuit which plays in important role in the design of the pre-charge circuit.

Figure 1
RC Circuit



The DC analysis of the circuit in Figure 1 is important for the pre-charge circuit to sustain functionality after the bulk load capacitor is charged. This includes utilizing the resistive divider so that $V_{GS(DC)}$ does not exceed the maximum value of the gate-to-source voltage for the chosen MOSFET. Standard values of R1 = 250kΩ and $V_{GS(DC)}$ = 9V should be used as a rule of thumb so that R2 can be easily calculated using the following equation.

$$R2 = \frac{R1}{\frac{V_{OUT}}{V_{GS(DC)}} - 1} \qquad (2)$$

The resistive divider also creates a Thevenin-Equivalent resistance that puts R1 and R2 in parallel with respect to C. The equivalent resistance is calculated as follows.

$$R_{TH} = \frac{1}{\frac{1}{R1} + \frac{1}{R2}} \qquad (3)$$

Another important aspect of the circuit in Figure 1 is the flexibility of the RC time constant τ. This time constant is defined by the time required to charge the capacitor by roughly 63.2% of its full potential. The value of τ is calculated in the following equation:

$$\tau = R_{TH} \bullet C \qquad (4)$$

When V_{OUT} is applied, a charging current is quickly passed through the capacitor C. As a result the instantaneous capacitor voltage, $V_{GS}(t)$, is derived as a function time.

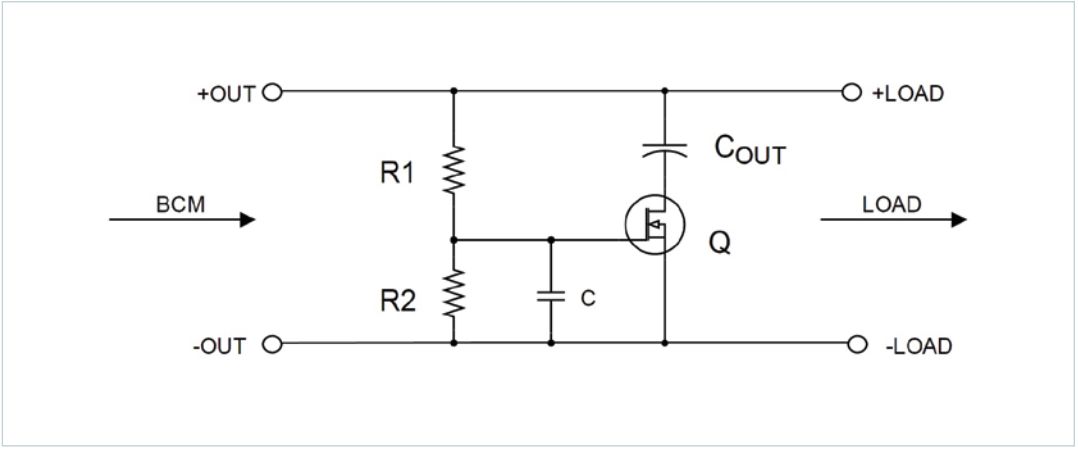
$$V_{GS}(t) = V_{GS(DC)}\left(1 - e^{-\frac{t}{\tau}}\right) \qquad (5)$$

Given V_{GS} as a function of time, the pre-charge circuit is nearly complete. Carefully choosing the values of R1, R2 and C will result in the capacitor arriving at a specified threshold voltage at an exact point in time. Thus, the BCM® is allotted a customized time interval to reach steady state, t_{CAP_DELAY}, before charging the bulk load capacitor.

Design Example

For this example we will use a BCM384P120T800ACR with a 12V output bus voltage. It is important to first note the startup specifications of BCMs to reach steady state found in the precise datasheet. ***Powertrain active to VAUX High***, t_{VAUX}, for this part number has a typical value of 2ms. We will use a steady state delay of t_{CAP_DELAY} = 5ms to ensure all startup cases are accounted for. Combining the proposed concepts of using a MOSFET and RC time constant arrives at the following circuit.

Figure 2
BCM Pre-charge Circuit



The first approach to the circuit Figure 2 should be selecting the appropriate resistive divider. As previously mentioned, the recommended R1 and $V_{GS(DC)}$ values are 250kΩ and 9V. Utilizing these values with Equation 2 equates R2 = 750kΩ. Thus, the Thevenin-Equivalent resistance computes to R_{TH} = 187.5kΩ using Equation 3.

After previously selecting the IRF510 MOSFET for Q, we will utilize its maximum threshold voltage specification of $V_{GS(TH)}$ = 4V. This threshold voltage will be set as the equivalent capacitor voltage, $V_{GS}(t)$, at time t_{CAP_DELAY} = 5ms, which is the desired point to start charging C_{OUT}. At this point we now have the following data:

$$t_{CAP\_DELAY} = 5ms, \qquad V_{GS}(5ms) = 4V, \qquad V_{GS(DC)} = 9V,$$

$$R1 = 250k\Omega, \qquad R2 = 750k\Omega, \qquad R_{TH} = 187.5k\Omega$$

Plugging the values stated above into Equation 5 yields the following steps:

$$4V = 9V\left(1 - e^{-\frac{5ms}{\tau}}\right)$$

$$e^{-\frac{5ms}{\tau}} = \left(1 - \frac{4}{9}\right)$$

$$-\frac{5ms}{\tau} = ln\left(\frac{5}{9}\right)$$

$$\tau = -\frac{5ms}{ln\left(\frac{5}{9}\right)}$$

$$\tau = 0.008506sec$$

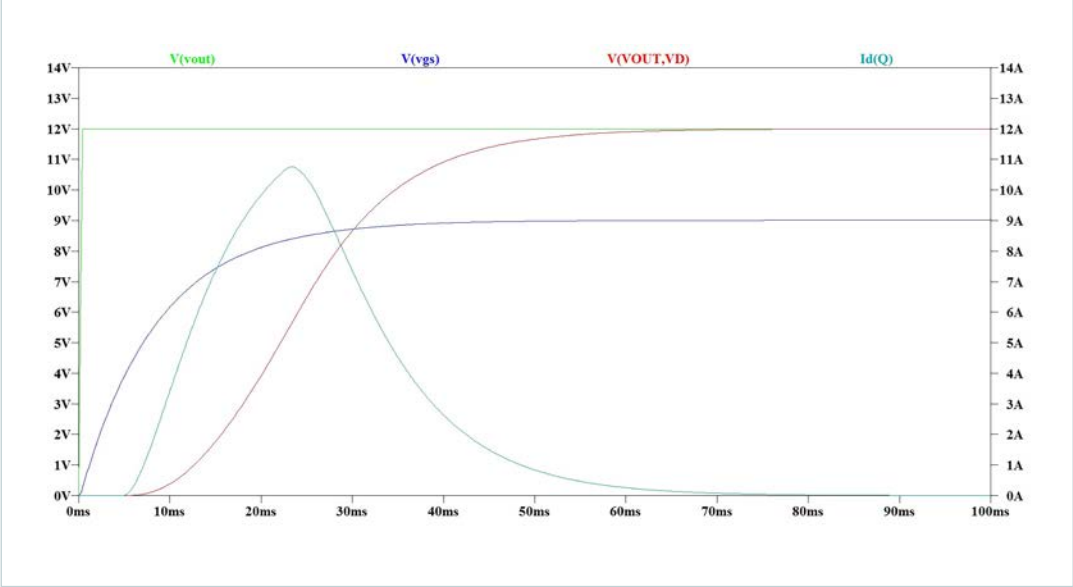
After solving for the desired time constant, Equation 4 can now be leveraged to choose a value for C.

$$0.008506sec = 187.5k\Omega \bullet C$$

$$C = 0.04536\mu F \approx 0.047\mu F$$

Now that the appropriate values have been chosen for Q, R1, R2 and C, the newly designed circuit can be evaluated.

Figure 3
5ms Delay Pre-Charge Waveform

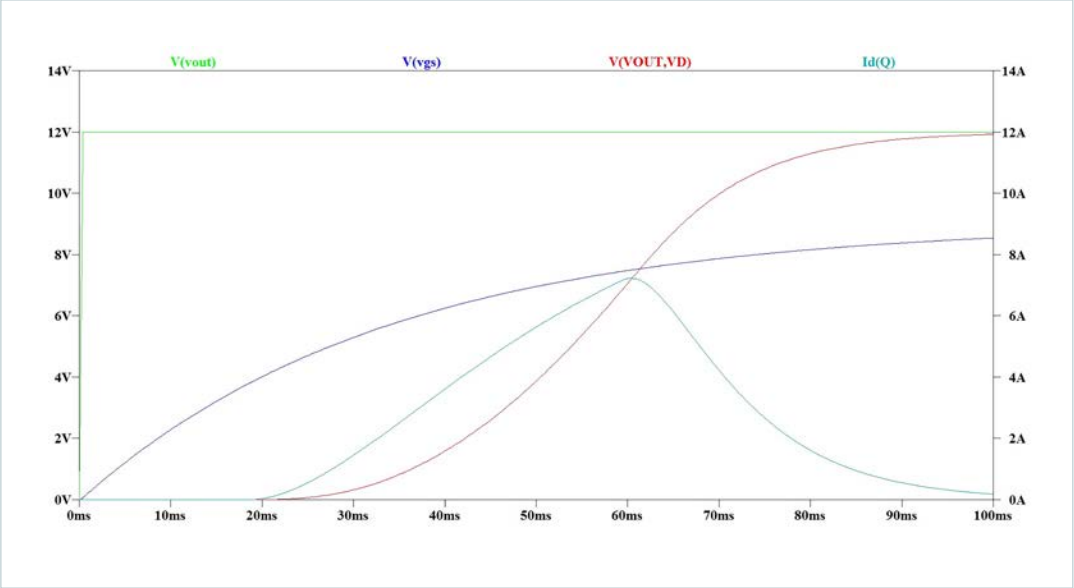


The above waveform is a result of an 18,000µF bulk load capacitance, which significantly exceeds the 1,000µF limit of the BCM384P120T800ACR. It can be observed that the desired 5ms delay was achieved at roughly V_{GS} = 4V. At this point, the charging current quickly flows through C_{OUT} and holds its differential voltage at the expected value of V_{OUT} = 12V. In this specific example the BCM384P120T800ACR is designed to output a maximum 68A of continuous current. While only reaching 11A of charging current in the waveform above, the BCM® should treat the instance as a load transient after passing the designed steady state delay.

Steady-State Delay

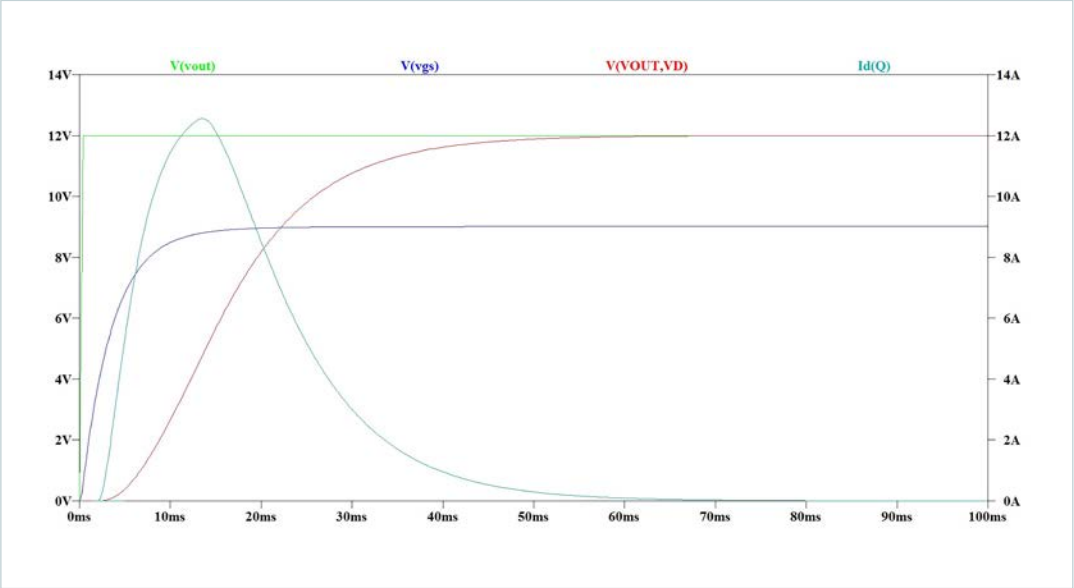
The example provided demonstrates the signal response of a 5ms steady state delay, but what happens if t_{CAP_DELAY} is modified?

Figure 4
20ms Delay
Pre-charge Waveform



The waveform in Figure 4 shows the response for using a 20ms delay for the circuit in Figure 2. A major difference between Figure 3 and Figure 4 is the peak charge current. The slow rise of V_{GS} in Figure 4 largely dictates the decreased drain current of the MOSFET.

Figure 5
2ms Delay
Pre-charge Waveform

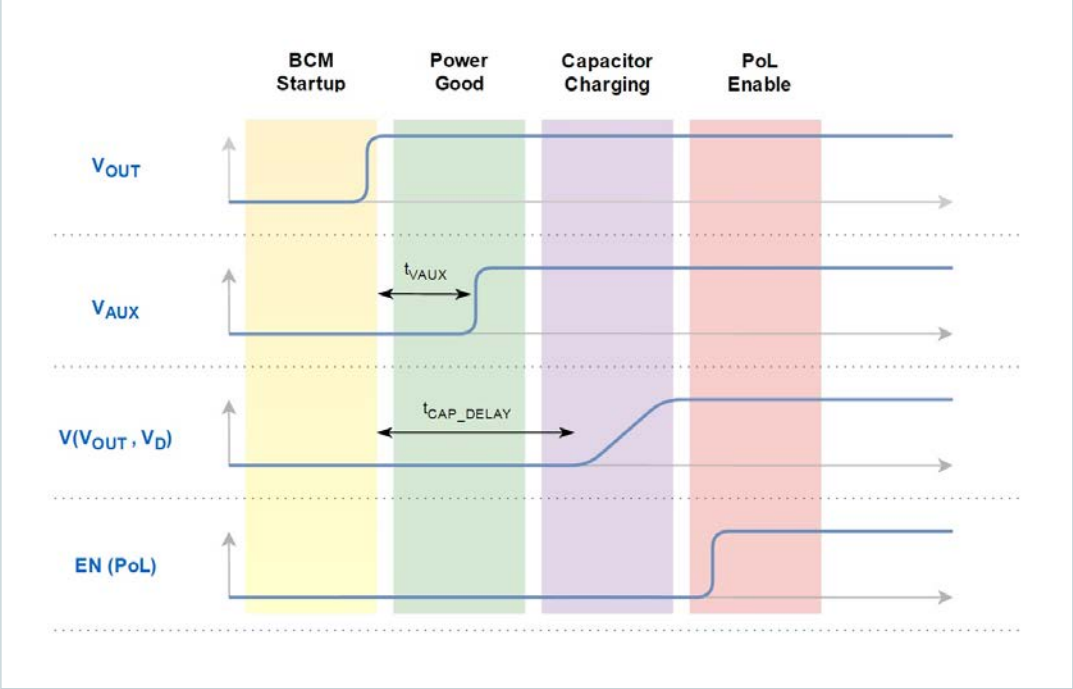


The waveform in Figure 5 shows the response for using a 2ms delay for the circuit in Figure 2. The smaller t_{CAP_DELAY} causes a steep voltage rise of V_{GS} followed by a larger peak drain current. As long as the peak charging current does not exceed the maximum pulsed drain current, I_{DM}, specification of the MOSFET the circuit shall remain functional. It is up to the designer to select a time constant that best fits the specific application.

Powering Point-of-Load Converters

A typical application of the pre-charge circuit is to charge the bulk input capacitance that is required with the use of downstream point-of-load (PoL) converters.

Figure 6
Timing Diagram for Powering Downstream PoL Converters



The timing diagram provided in Figure 6 should be used to delay the PoL start up until the bulk capacitance is charged. This is because most converters require input capacitance during start up for stability purposes. However the bulk capacitance is initially not present while the load line has already reached the desired bus voltage. If this delay is not in place the PoL start up may be unstable.

Another means for ensuring PoL start up stability is to integrate two types of capacitors. A large bulk capacitance can be used with the designed pre-charge circuit to execute hold-up events. Other small capacitors that are within the specifications of the BCM® could be used separate from the pre-charge circuit that immediately become charged and provide the necessary start up support.

Discharging

Another important aspect to consider of the pre-charge circuit is how the bulk capacitor discharges while the load is still on. When the capacitor discharges the body diode of the MOSFET becomes forward-biased and a current is quickly passed through it. It is crucial that the peak discharge current does not exceed the maximum-pulsed current of the body diode, I_{SM}, within the MOSFET.

For example, a BCM has a 12V output bus and is powering a 300W constant-power PoL converter. Additionally, the specific PoL has an undervoltage lockout (UVLO) turnoff of 8V. Therefore, the maximum discharge current for this specific application is computed as follows.

$$I_{SM(MAX)} = \frac{300W}{8V} \approx 37.5A$$

In this case, the maximum discharge current is larger than the maximum pulsed diode forward current of the IRF510, which has a value of 20A. For this specific application we would need to select a new MOSFET with a higher current rating, or place another MOSFET in parallel with Q in order for the pre-charge circuit to remain functional.

Guidelines

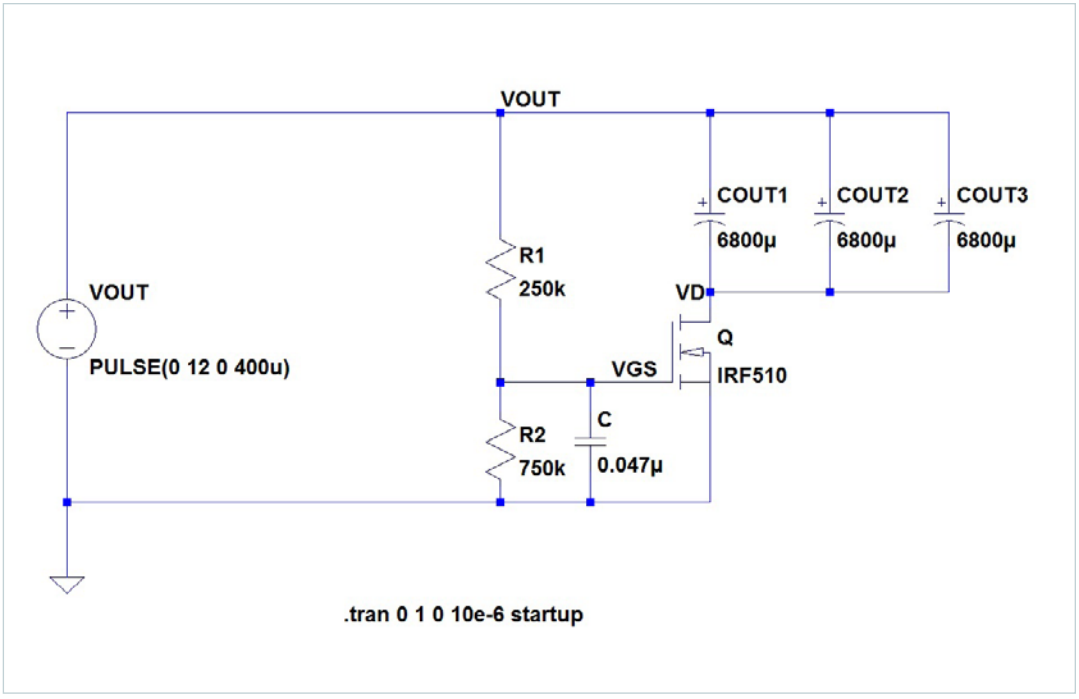
- Refer to the datasheet of the corresponding BCM® part number being used in order to obtain the necessary information.
- To obtain the same delay response as in the design example, start with using R1 = 250kΩ, $V_{GS(DC)}$ = 9V, t_{CAP_DELAY} = 5ms and = 0.01233 as fixed values and the same MOSFET. Then R2 and C are calculated as follows:

$$R2 = \frac{R1}{\frac{V_{OUT}}{V_{GS(DC)}} - 1}$$

$$C = \tau \left(\frac{1}{R1} + \frac{1}{R2} \right)$$

- Actual peak-charging current will vary from simulation value, and it should not exceed the maximum I_{DM} of the MOSFET. It is recommended to use the exhibited IRF510 or N-Channel power MOSFET type.
- If the BCM is powering downstream PoL converters, it is recommended to delay the PoL start up until the bulk capacitance is charged. Another means for ensuring PoL start up stability is to integrate two types of capacitors.
- Discharging current should not exceed the maximum I_{SM} of the chosen MOSFET. Designer may need to select a MOSFET with a high enough current rating or place multiple MOSFETs in parallel with Q.
- Simulating the pre-charge circuit may assist designers with optimizing a custom solution. [1]

Figure 7
LTspice Simulated Pre-charge Circuit

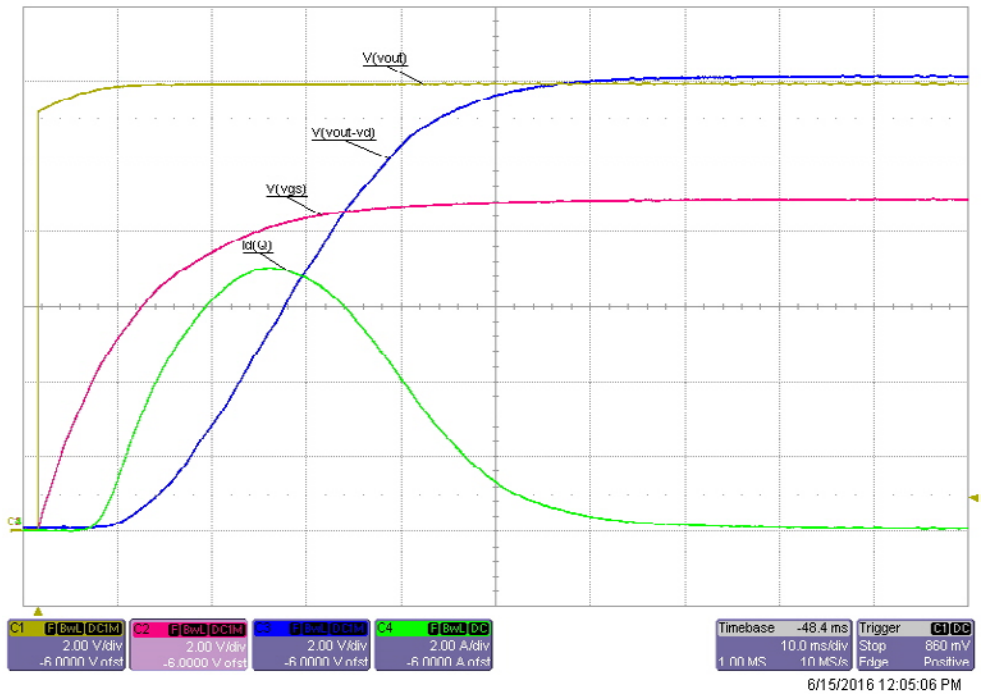


[1] To view this example, please dowload the following circuit: LTspice IV Circuit Simulation Example

Experimental Results

The experiment was performed using the BCM384P120T800ACR to validate the proposed solution.

Figure 8
Experimental Results
5ms Delay
Pre-charge Waveform



Conclusion

A circuit was demonstrated with precise recommendations to allow BCMs® to operate with an external load capacitance beyond the maximum specification. The simplicity of the proposed solution accommodates for special applications that deploy BCMs to power a factorized bus or individual point-of-load. Moreover, the proposed solution does not disrupt the main power path which would need to be rated for higher current and would likely be costly, big, inefficient and difficult to cool. Utilizing the fundamentals of hardware with the addition of just four low cost components eliminates the need to redesign an entire power system.

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