



## 48V to Point-of-Load Non-Isolated, Regulated DC Converter

### Features & Benefits

- Wide input range 40 – 60V<sub>DC</sub>
- Trimmable output range 10.0 – 12.5V<sub>DC</sub>
- 96.5% peak efficiency
- Up to 750W continuous operation
- Up to 900W or 74A transient peak
- >1MHz switching frequency
- PMBus® compatible telemetry
- Internal voltage, current and temperature shut down
- Array configuration of up to four units

### Typical Applications

- Data Center Applications
- High-Performance Computing Systems (HPC)
- Mild-Hybrid and Autonomous Vehicles
- Industrial Systems

### Product Ratings

$V_{IN} = 40 - 60V$	$P_{OUT} = 750W$
$V_{OUT} = 12.2V$ Nominal (10.0 – 12.5V)	$I_{OUT} = 61.5A$ (Max)

### Product Description

The DCM3717 is a non-isolated, regulated DC-DC converter module that operates from a semi-regulated 40 – 60V input to generate a regulated point-of-load output with a voltage range of 10.0 – 12.5V. The DCM3717 in the SM-ChiP package configuration utilizes the Vicor patented zero-voltage switching (ZVS) buck-boost regulator stage followed by the Sine Amplitude Converter (SAC™).

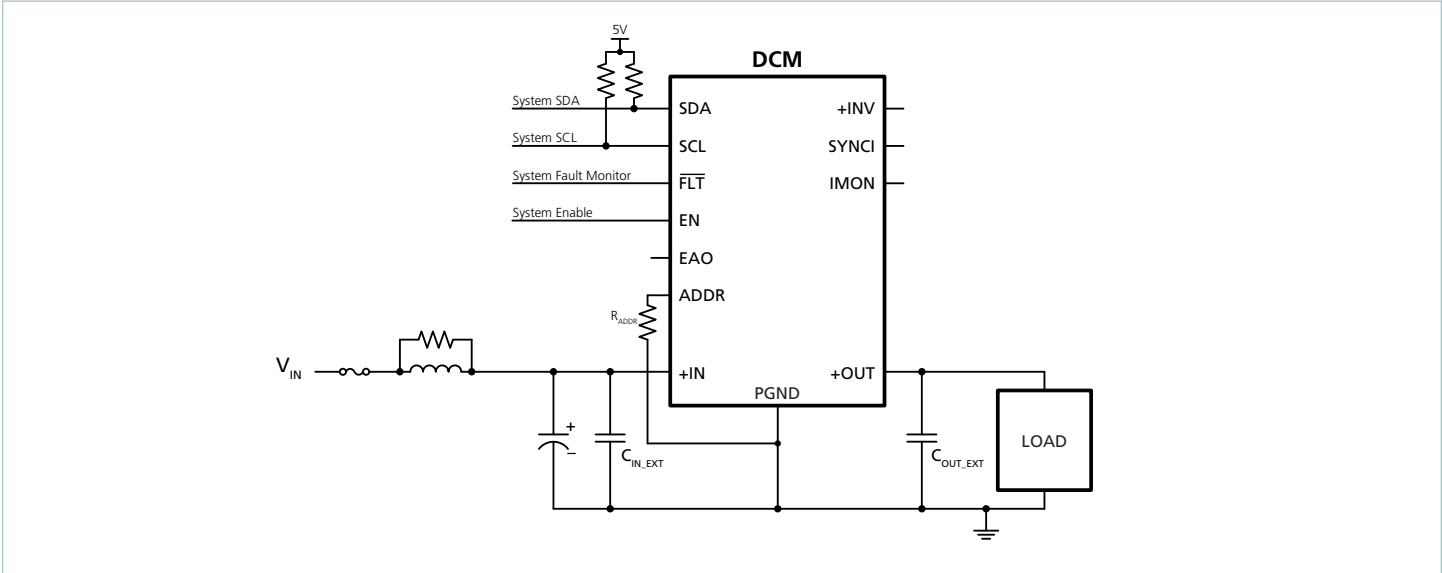
Leveraging Vicor SM-ChiP packaging technology, the DCM offers flexible thermal management options with very low top- and bottom-side thermal impedances. Thermally adept SM-ChiP-based power components enable customers to achieve low-cost power system solutions with previously unattainable system size, weight and efficiency attributes quickly and predictably.

### Package Information

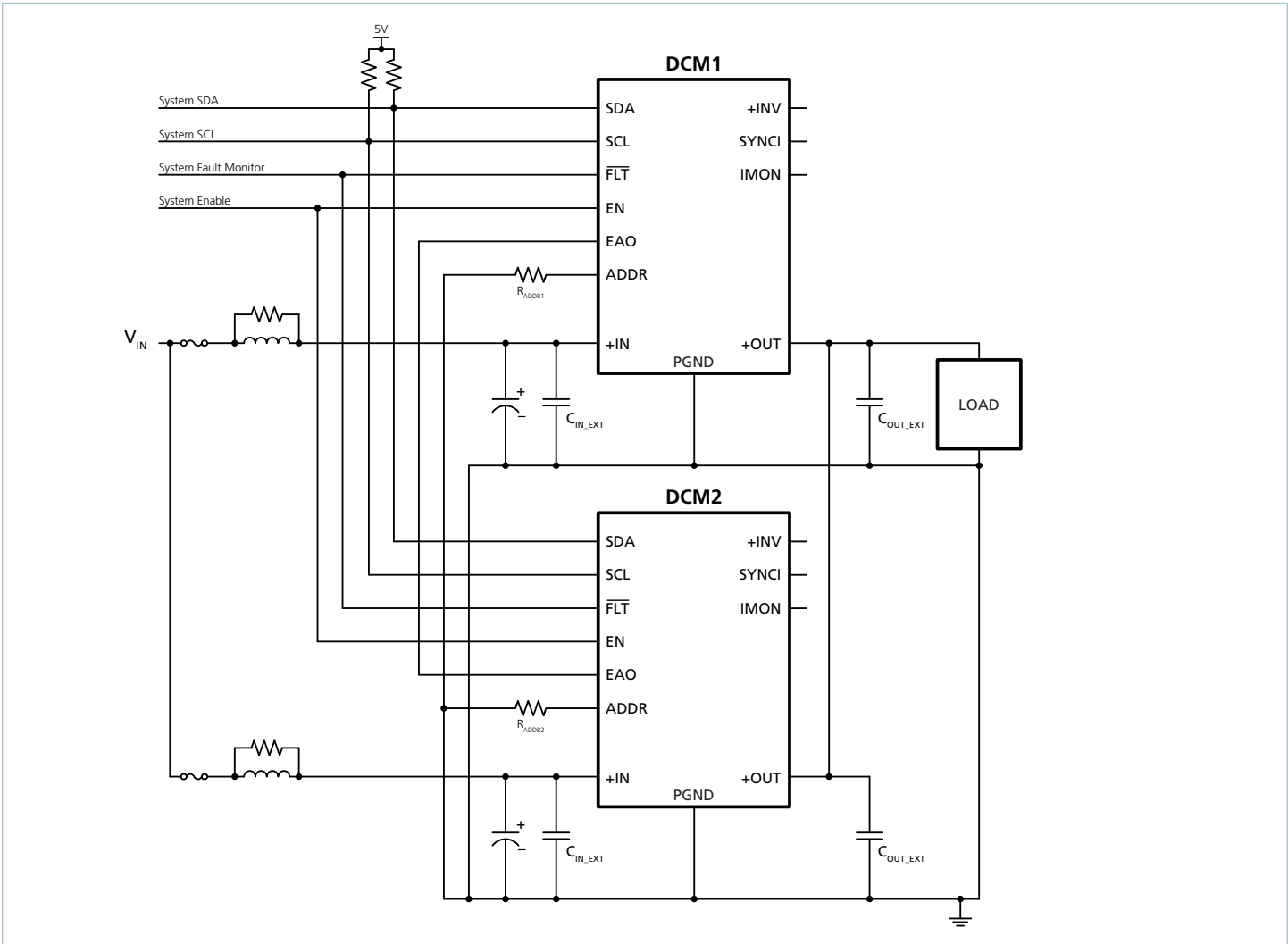
- 36.7 x 17.3 x 5.2mm SM-ChiP™
- Weight: 14.3g

Note: Product images may not highlight current product markings and cosmetic features.

Typical Applications

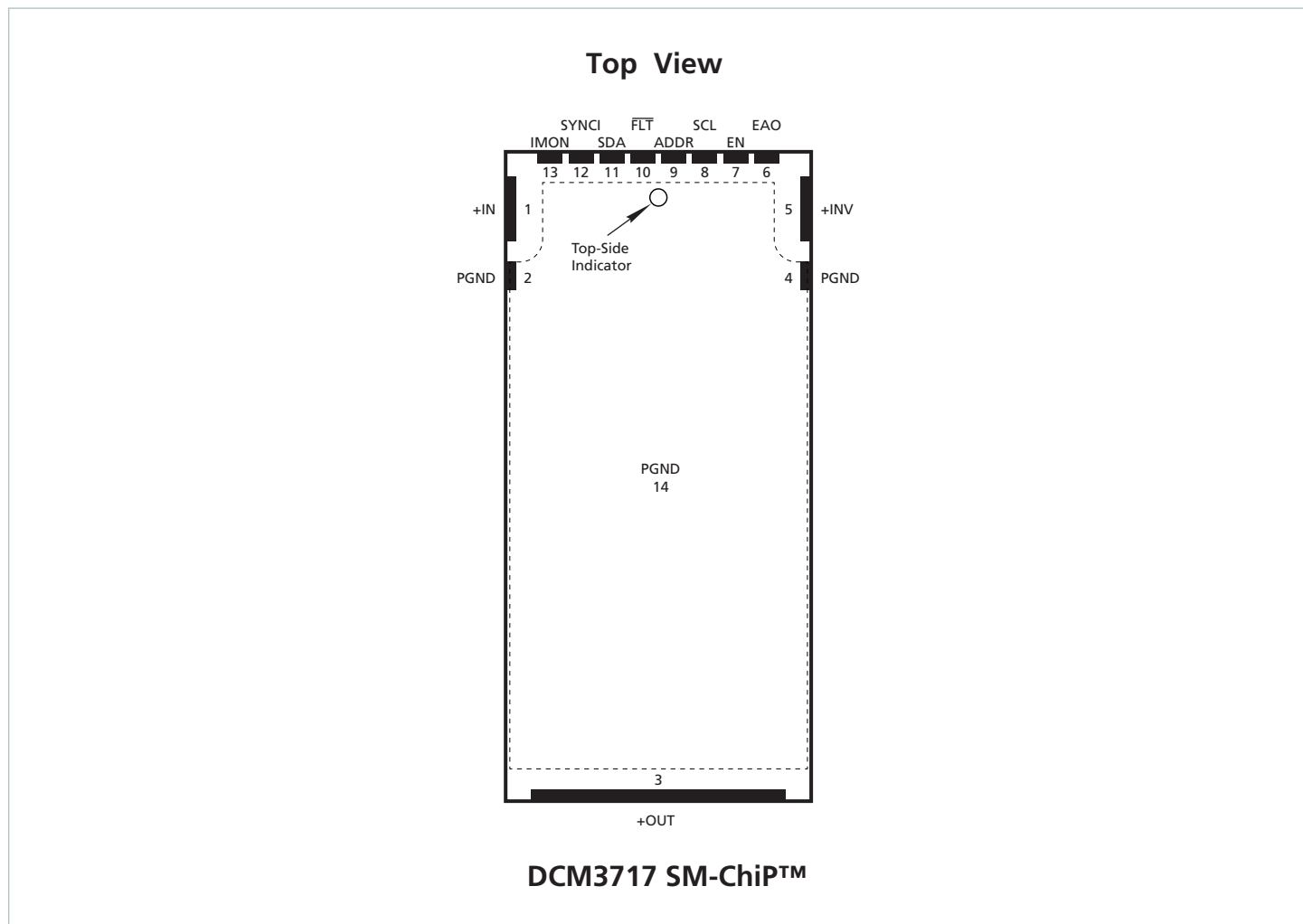


DCM3717 to point-of-load



DCM3717s in a high-power array

## Terminal Configuration



## Terminal Descriptions

Signal Name	Terminal Number	Terminal Functions
+IN	1	Positive Input: power terminal
PGND	2, 4, 14 <sup>[a]</sup>	Power Ground: power return for +IN and +OUT current
+OUT	3	Positive Output: power terminal
+INV	5	Positive Intermediate: power terminal
EAO	6	Transconductance error amplifier output and powertrain modulator control node
EN	7	Enable: when input asserted active or left floating, regulator is enabled
SCL	8	Digital serial communication clock terminal
ADDR	9	Digital serial communication address assignment
$\overline{\text{FLT}}$ <sup>[b]</sup>	10	Fault Flag: pulled low when a fault is detected
SDA	11	Digital serial communication data terminal
SYNCI	12	Factory use only
IMON	13	Factory use only

<sup>[a]</sup> Terminal 14 represents the package top and bottom conductive plating. Refer to product outline for additional details.

<sup>[b]</sup> Overbar ( $\overline{\text{FLT}}$ ) or star ( $\text{FLT}^*$ ) marking signify an active low designation.

## Part Ordering Information

Part Number	Temperature Grade	Tray Size
DCM3717S60E13G5TN1	T = -40 to 125°C	323 x 136 x 12mm 24 parts per tray Vicor PN 48695

## Storage and Handling Information

**Note:** For compressive loading refer to [Application Note AN:036](#), "Recommendations for Maximum Compressive Force of Heat Sinks." For handling and assembly processing, and for rework considerations refer to [Application Note AN:701](#), "SM-ChiP Reflow Soldering Recommendations."

Attribute	Comments	Specification
Storage Temperature Range		-40 to 125°C
Operating Internal Temperature Range	Temperature at the hottest internal component (T <sub>INT</sub> ) must not exceed this maximum	-40 to 125°C
Weight		14.3g
Package Plating		75µm copper with ENiG surface finish
MSL Rating		MSL 4, 245°C maximum reflow temperature
ESD Rating	Human Body Model JEDEC JS-001-2012	Class 2, ≥ 2000V to < 8000V
	Charged Device Model JESD22C101-E	Class 2, ≥ 200V to < 500V

## Reliability and Agency Approvals

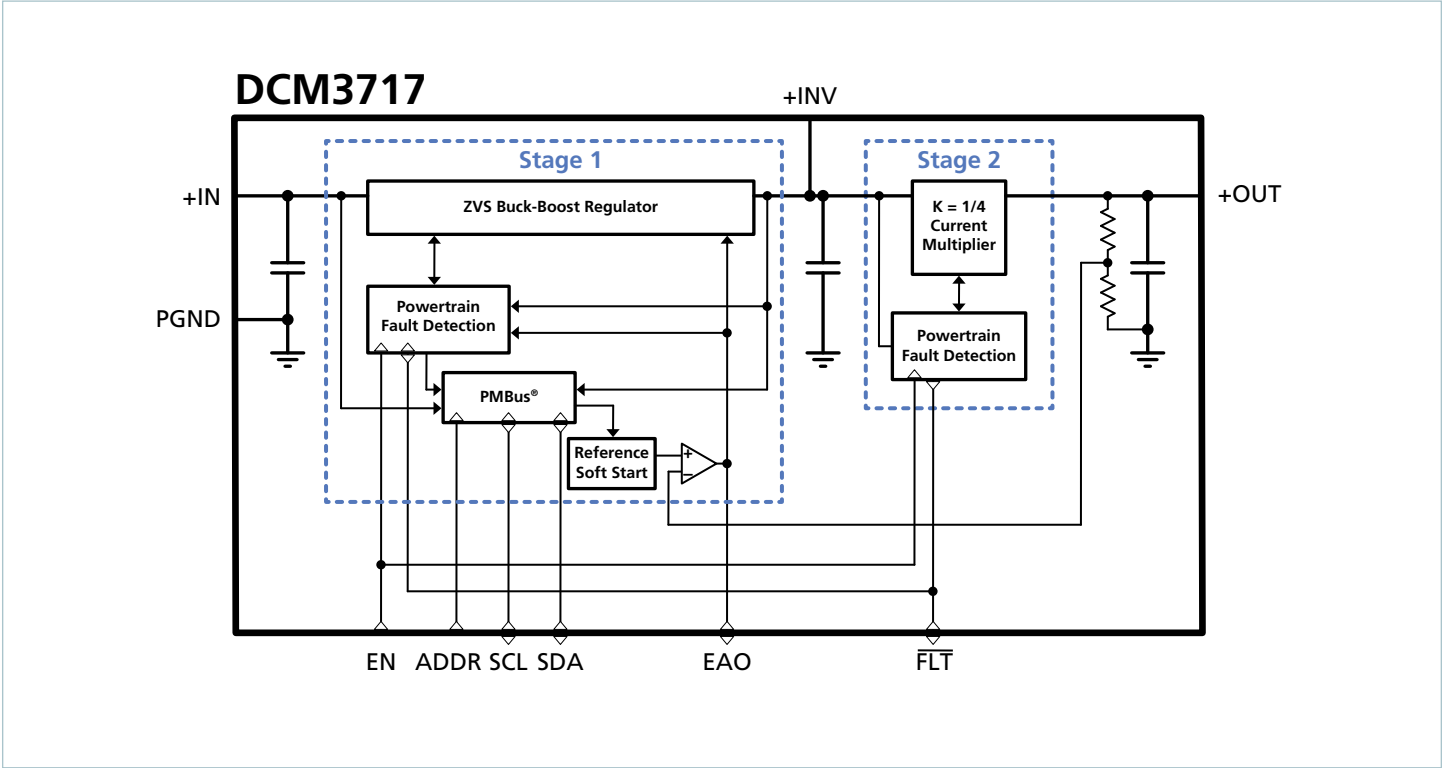
Attribute	Comments	Value	Unit
MTBF	Telcordia SR-332 Issue 2, Method I Case 3, Ground Benign	20	MHrs
	MIL-HDBK-217F Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer	9	
Agency Approvals/Standards	cTÜVus EN IEC 62368-1, UL 62368-1, CSA-C22.2 No. 62368-1		
	UKCA, electrical equipment (safety) regulations		
	CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable		

## Absolute Maximum Ratings

The ABSOLUTE MAXIMUM ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to device. Electrical specifications do not apply when operating beyond rated operating conditions. Operating beyond rated operating conditions for an extended period of time may affect device reliability. All voltages referenced to PGND. Positive terminal currents represent current flowing out of the terminal.

Parameter	Comments	Min	Max	Unit
+IN	Non-operating	-0.3	70	V
+OUT	Continuous, non-operating	-0.3	15	V
		-120	120	A
+INV	Non-operating	-0.3	60	V
		-40	40	A
EAO		-0.3	5.5	V
EN		-0.3	5.5	V
SCL, SDA, ADDR		-0.3	5.5	V
$\overline{\text{FLT}}$		-0.3	5.5	V
		-20	20	mA

Functional Block Diagram



## Electrical Characteristics

Specifications apply over all line, trim, and load conditions unless otherwise noted. Boldface specifications apply over the temperature range of  $-40^{\circ}\text{C} \leq T_{\text{INT}} \leq 125^{\circ}\text{C}$  and are assured to meet performance specification by design, test correlation, characterization and/or statistical process control. All other specifications are at  $T_{\text{INT}} = 25^{\circ}\text{C}$  unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
<b>Powertrain Input Specifications</b>						
Input Voltage Range	$V_{\text{IN}}$	Continuous, operating	<b>40.0</b>	54.0	<b>60.0</b>	V
Input Voltage Slew Rate	$dV_{\text{IN}}/dt$				1	V/ $\mu\text{s}$
Input Voltage for ADDR Latch	$V_{\text{IN\_ADDR}}$	Initial power up			<b>12</b>	V
No-Load Input Power	$P_{\text{NL}}$	ENABLE HIGH, $V_{\text{IN}} = 54.0\text{V}$ , $V_{\text{OUT}} = 12.2\text{V}$		5.1	<b>8.5</b>	W
Input Quiescent Current	$I_{\text{QC}}$	ENABLE LOW, $V_{\text{IN}} = 54.0\text{V}$		7.6	<b>10.4</b>	mA
Input Current	$I_{\text{IN\_DC}}$	$I_{\text{OUT}} = 61.5\text{A}$ , $V_{\text{IN}} = 54.0\text{V}$ , $V_{\text{OUT}} = 12.2\text{V}$		14.4	<b>15</b>	A
Input Capacitance (Internal)	$C_{\text{IN\_INT}}$	Effective value, $V_{\text{IN}} = 54.0\text{V}$		3.6		$\mu\text{F}$
Input Capacitance (Internal) ESR	$R_{\text{CIN\_INT}}$	Effective value, $V_{\text{IN}} = 54.0\text{V}$		0.46		m $\Omega$
<b>Powertrain Output Specifications</b>						
Output Voltage Set Point	$V_{\text{OUT\_SET}}$	No load; typical value lists product nominal $V_{\text{OUT}}$	<b>12.07</b>	12.2	<b>12.32</b>	V
Output Voltage Trim Range	$V_{\text{OUT}}$		<b>10.0</b>		<b>12.5</b>	V
Output Voltage Load Regulation	$V_{\text{OUT-REG-LOAD}}$	For load > 10%		0.1	<b>0.3</b>	%
Output Voltage Line Regulation	$V_{\text{OUT-REG-LINE}}$			0.1	<b>0.2</b>	%
Total Regulation Error	$V_{\text{OUT-REG-TOTAL}}$	For load > 10%			<b>0.5</b>	%
Rated Output Current, Continuous	$I_{\text{OUT}}$	$V_{\text{OUT}} \leq 12.2\text{V}$			<b>61.5</b>	A
Rated Output Power, Continuous	$P_{\text{OUT}}$	$12.2\text{V} \leq V_{\text{OUT}}$			<b>750</b>	W
Rated Output Current, Peak	$I_{\text{OUT\_PK}}$	$V_{\text{OUT}} \leq 12.2\text{V}$ , $\leq 1\text{ms}$ pulse width, $\leq 10\%$ duty cycle			<b>73.8</b>	A
Rated Output Power, Peak	$P_{\text{OUT\_PK}}$	$12.2\text{V} \leq V_{\text{OUT}} \leq 12.5\text{V}$ , $\leq 1\text{ms}$ pulse width, $\leq 10\%$ duty cycle			<b>900</b>	W
Array Size	$n_{\text{ARRAY}}$				<b>4</b>	DCMs
Switching Frequency, Buck-Boost Stage 1	$F_{\text{SW1}}$	$V_{\text{IN}} = 54.0\text{V}$ , $V_{\text{OUT}} = 12.2\text{V}$ , $I_{\text{OUT}} = 61.5\text{A}$	0.5	0.63	0.80	MHz
		Over rated line, continuous load, trim and temperature, exclusive of pulse-skip mode	<b>0.35</b>		<b>1.7</b>	
Switching Frequency, Current Multiplier Stage 2	$F_{\text{SW2}}$	$V_{\text{IN}} = 54.0\text{V}$ , $V_{\text{OUT}} = 12.2\text{V}$ , $I_{\text{OUT}} = 61.5\text{A}$	1.7	1.75	1.8	MHz
		Over rated line, continuous load, trim and temperature	<b>1.57</b>		<b>1.95</b>	
Transfer Ratio, Current Multiplier Stage 2	K			1/4		V/V
Minimum Off Time to Restart	$t_{\text{OFF}}$	When externally disabled with EN or $\overline{\text{FLT}}$ terminal			<b>500</b>	$\mu\text{s}$
Off Time for Monotonic Restart	$t_{\text{OFF-MONO}}$	Extend disable time with EN or $\overline{\text{FLT}}$			<b>15</b>	s
Output Turn-On Delay	$t_{\text{ON}}$	From EN release to soft-start ramp, $V_{\text{IN}}$ pre-applied		800		$\mu\text{s}$
Output Voltage Rise Time	$t_{\text{SS}}$	From soft start begin to $V_{\text{OUT}}$ settled to within 5% for nominal $V_{\text{OUT}}$	<b>6</b>	10	<b>16</b>	ms
Output Voltage Soft-Start Slew Rate	$dV_{\text{OUT}}/dt$	All rated $V_{\text{OUT}}$ trim range	0.47	0.76	1.1	V/ms
Efficiency, Ambient	$\eta_{\text{AMB}}$	$V_{\text{IN}} = 54.0\text{V}$ , $V_{\text{OUT}} = 12.2\text{V}$ , $I_{\text{OUT}} = 61.5\text{A}$ , $T_{\text{CASE}} = 25^{\circ}\text{C}$	95.8	96.1		%
		$V_{\text{IN}} = 54.0\text{V}$ , $V_{\text{OUT}} = 12.2\text{V}$ , $I_{\text{OUT}} = 31\text{A}$ , $T_{\text{CASE}} = 25^{\circ}\text{C}$	95.6	96.0		
		$V_{\text{IN}} = 40.0 - 60.0\text{V}$ , $V_{\text{OUT}} = 12.2\text{V}$ , $I_{\text{OUT}} = 31\text{A}$ , $T_{\text{CASE}} = 25^{\circ}\text{C}$	94			
		$V_{\text{IN}} = 40.0 - 60.0\text{V}$ , $I_{\text{OUT}} = \text{max rated}$ , $T_{\text{CASE}} = 25^{\circ}\text{C}$ , over trim	93.6			
Efficiency Over Temperature	$\eta$	$V_{\text{IN}} = 40.0 - 60.0\text{V}$ , $V_{\text{OUT}} = 12.2\text{V}$ , >50% rated load current, over temperature	<b>93.6</b>			%
		$V_{\text{IN}} = 40.0 - 60.0\text{V}$ , >50% rated load current, over temperature and trim	<b>93.4</b>			

## Electrical Characteristics (Cont.)

Specifications apply over all line, trim, and load conditions unless otherwise noted. Boldface specifications apply over the temperature range of  $-40^{\circ}\text{C} \leq T_{\text{INT}} \leq 125^{\circ}\text{C}$  and are assured to meet performance specification by design, test correlation, characterization and/or statistical process control. All other specifications are at  $T_{\text{INT}} = 25^{\circ}\text{C}$  unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
<b>Powertrain Output Specifications (Cont.)</b>						
Output Voltage Ripple	$V_{\text{OUT\_PP}}$	$V_{\text{IN}} = 54.0\text{V}$ , $V_{\text{OUT}} = 12.2\text{V}$ , $I_{\text{OUT}} = 61.5\text{A}$ , $C_{\text{OUT\_EXT}} = 69\mu\text{F}$ effective, 20MHz BW		100		mV <sub>P-P</sub>
Output Capacitance (Internal)	$C_{\text{OUT\_INT}}$	Effective value, $V_{\text{OUT}} = 12.2\text{V}$		33.3		$\mu\text{F}$
Output Capacitance (Internal) ESR	$R_{\text{COUT\_INT}}$	Effective value, $V_{\text{OUT}} = 12.2\text{V}$		0.29		m $\Omega$
Load Capacitance (Bulk)	$C_{\text{LOAD\_BULK}}$	Per DCM, ESR > 2m $\Omega$	<b>0</b>		<b>10</b>	mF
Load Capacitance (Ceramic)	$C_{\text{LOAD\_CER}}$	Per DCM	<b>0</b>		<b>200</b>	$\mu\text{F}$
Load Capacitance (Total)	$C_{\text{LOAD\_TOTAL}}$	Per DCM	<b>0</b>		<b>10</b>	mF
Load Transient Voltage Deviation	$V_{\text{TRANS}}$	10 $\leftrightarrow$ 100% load step, 10A/ $\mu\text{s}$ , $C_{\text{OUT\_EXT}} = 8 \times 22\mu\text{F}$ ceramic (69 $\mu\text{F}$ effective) per DCM and 2200 $\mu\text{F}$ aluminum for the array; $V_{\text{OUT\_SET}} = 12.2\text{V}$ , $n_{\text{ARRAY}} = 4$		$\pm 500$		mV
Load Transient Recovery Time	$t_{\text{TRANS}}$	10 $\leftrightarrow$ 100% load step, 10A/ $\mu\text{s}$ , $C_{\text{OUT\_EXT}} = 8 \times 22\mu\text{F}$ ceramic (69 $\mu\text{F}$ effective) per DCM and 2200 $\mu\text{F}$ aluminum for the array; $V_{\text{OUT\_SET}} = 12.2\text{V}$ , $n_{\text{ARRAY}} = 4$ ; to within $\pm 0.5\%$ $V_{\text{OUT}}$ steady-state value		50		$\mu\text{s}$
<b>Fault Detection and Response</b>						
Input Undervoltage Turn-ON	$V_{\text{IN\_UVLO+}}$	Powertrain recovery	<b>36.1</b>	37.4	<b>38.3</b>	V
Input Voltage UVLO Hysteresis	$V_{\text{IN\_UVLO\_HYS}}$	Powertrain shut down	<b>1.5</b>	1.9	<b>2.2</b>	V
Input Overvoltage Turn-OFF	$V_{\text{IN\_OVLO+}}$	Powertrain shut down	<b>62.3</b>	64.7	<b>67.1</b>	V
Input Voltage OVLO Hysteresis	$V_{\text{IN\_OVLO\_HYS}}$	Powertrain recovery	<b>1.7</b>	2.3	<b>3</b>	V
Overtemperature Shut Down	$T_{\text{OT}}$	Detected at stage-1 control IC	<b>125</b>			$^{\circ}\text{C}$
Overtemperature Restart Hysteresis	$T_{\text{OT\_HYS}}$	Measured at stage-1 control IC		18		$^{\circ}\text{C}$
EAO Overload	$V_{\text{EAO\_OL}}$		<b>3.2</b>	3.3		V
EAO Overload Timeout	$t_{\text{EAO\_OL}}$	EAO continuously above $V_{\text{EAO\_OL}}$		1000		$\mu\text{s}$
Output Voltage Negative Fault Threshold	$V_{\text{OUT\_NEG}}$	Level threshold to trigger fault	<b>-0.45</b>	-0.25	<b>-0.15</b>	V
Output Voltage Threshold to Re-Enable $V_{\text{OUT\_NEG}}$ Fault	$V_{\text{OUT\_NEG\_RE-ARM}}$	Positive-going $V_{\text{OUT}}$ which re-arms the $V_{\text{OUT\_NEG}}$ fault	<b>1</b>	2.25	<b>3</b>	V
Overcurrent Shut Down	$I_{\text{OC}}$	$I_{\text{OC1}}$ when detected by ZVS buck-boost stage; $I_{\text{OC2}}$ when detected by current multiplier stage	<b>68</b>	87		A
Overcurrent Timeout	$t_{\text{IOC}}$	Output current above $I_{\text{OC}}$	<b>1</b>	4		ms
Short Circuit Shut Down	$I_{\text{SHORT}}$			96		A
Output OVP Turn-OFF	$V_{\text{OUT\_OVP}}$	Relative to module +INV terminal	<b>56.5</b>		<b>58</b>	V
Output OVP Relative	$\%E_{\text{AIN\_HI}}$	Relative to the $V_{\text{OUT\_COMMAND}}$ ; inactive during start up and for $t_{\text{EAIN\_HI}}$ after a $V_{\text{OUT\_COMMAND}}$	<b>4</b>	15		%
Output OVP Relative Timeout	$t_{\text{EAIN\_HI}}$	Blanking time for output OVP relative shut down following $V_{\text{OUT\_COMMAND}}$		2.1		s
Fault Response Time	$t_{\text{FAULT}}$	Excluding $t_{\text{EAO\_OL}}$ and $t_{\text{IOC}}$ timeout periods		1		$\mu\text{s}$
Stage 1 Fault Recovery Time	$t_{\text{FAULT1\_RECOVERY}}$	Excluding $I_{\text{OC2}}$ and $T_{\text{OT}}$ shut downs	35	40	45	ms
Stage 2 Fault Recovery Time	$t_{\text{FAULT2\_RECOVERY}}$	Recovery from stage-2 multiplier OVP, IOC and $I_{\text{SHORT}}$ shut downs only		140		ms

## Electrical Characteristics (Cont.)

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Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
<b>PMBus® Characteristics</b>						
READ_VIN Accuracy	$V_{\text{READ\_VIN\_ACC}}$	At nominal $V_{\text{IN}}$	-5		5	%
READ_VIN Resolution	$V_{\text{READ\_VIN\_RES}}$	Limited to PMBus READ_VIN format resolution		125		mV
VOUT_COMMAND Resolution	$V_{\text{VOUT\_CMD\_RES}}$			1.95		mV
READ_VOUT Accuracy	$V_{\text{READ\_VOUT\_ACC}}$	At nominal trim, +INV referred	-5		5	%
READ_VOUT Resolution	$V_{\text{READ\_VOUT\_RES}}$			1.95		mV
READ_IOUT Functional Range	$V_{\text{READ\_IOUT\_RNG}}$		<b>0</b>		<b>70</b>	A
READ_IOUT Accuracy, Ambient	$V_{\text{READ\_IOUT\_ACC}}$	$V_{\text{IN}} = 40.0 - 60.0\text{V}$ , >50% rated load current, $T_{\text{CASE}} = 25^{\circ}\text{C}$ , over trim	-7.5		7.5	%
		$V_{\text{IN}} = 40.0 - 60.0\text{V}$ , >50% rated load current, over temperature and trim	<b>-7.5</b>		<b>20</b>	%
READ_IOUT Resolution	$V_{\text{READ\_IOUT\_RES}}$			250		mA
READ_TEMPERATURE Accuracy	$V_{\text{READ\_TEMP\_ACC}}$	Disabled, with $T_{\text{CASE}} = 25^{\circ}\text{C}$	-6		6	$^{\circ}\text{C}$
PMBus Operating Frequency Range	$f_{\text{PMBUS}}$	Child mode			<b>400</b>	kHz
STORE_USER_CODE Capacity	$N_{\text{STORE\_USER\_CODE}}$	Permanent storage of VOUT_COMMAND	<b>8</b>			Writes
<b>Control Node: EAO</b>						
EAO Voltage Range	$V_{\text{EAO}}$		<b>0</b>		<b>3.15</b>	V
EAO Current Drive	$I_{\text{EAO}}$		<b>300</b>		<b>600</b>	$\mu\text{A}$
EAO Pulse Skip Threshold	$V_{\text{EAO\_SKIP}}$	Lower side of hysteretic range		0.4		V
Output Current Pulse Skip Threshold	$\%I_{\text{OUT\_SKIP}}$	Percentage of $I_{\text{OUT}}$ at $V_{\text{IN}} = 54\text{V}$		20		%
EAO Sink Current	$I_{\text{EAO\_FAULT}}$	Pull down to 0V while shut down due to a fault		450		$\mu\text{A}$
<b>Enable: EN</b>						
EN Input High Voltage	$V_{\text{EN\_HIGH}}$		<b>1.1</b>			V
EN Input Low Voltage	$V_{\text{EN\_LOW}}$				<b>0.7</b>	V
EN Source Current	$I_{\text{EN}}$	Pull up to ~5V			200	$\mu\text{A}$
<b>Serial Clock: SCL Serial Data: SDA</b>						
Rated Input Range	$V_{\text{SERIAL}}$		<b>0</b>		<b>5</b>	V
SCL Frequency	$F_{\text{SCL}}$		<b>100</b>		<b>400</b>	kHz
Input High Voltage	$V_{\text{IH}}$		<b>1.35</b>			V
Input Low Voltage	$V_{\text{IL}}$				<b>0.8</b>	V
Output Low Voltage	$V_{\text{OL}}$	Sinking 4mA			<b>0.4</b>	V
<b>Address: ADDR</b>						
Address Registration Delay	$t_{\text{ADDR\_DLY}}$	From $V_{\text{IN}}$ crossing $V_{\text{IN\_ADDR}}$		10.5	<b>30</b>	ms
<b>Fault: FLT</b>						
Fault Input High Voltage	$V_{\text{FLT\_IN\_HIGH}}$		<b>1.15</b>			V
Fault Input Low Voltage	$V_{\text{FLT\_IN\_LOW}}$	To externally induce shut down			<b>0.85</b>	V
Fault Output Low Voltage	$V_{\text{FLT\_OUT\_LOW}}$	$I_{\text{FLT}} = 4\text{mA}$			<b>0.4</b>	V



### Specified Operating Area

The following figures present performance data in a typical application environment.

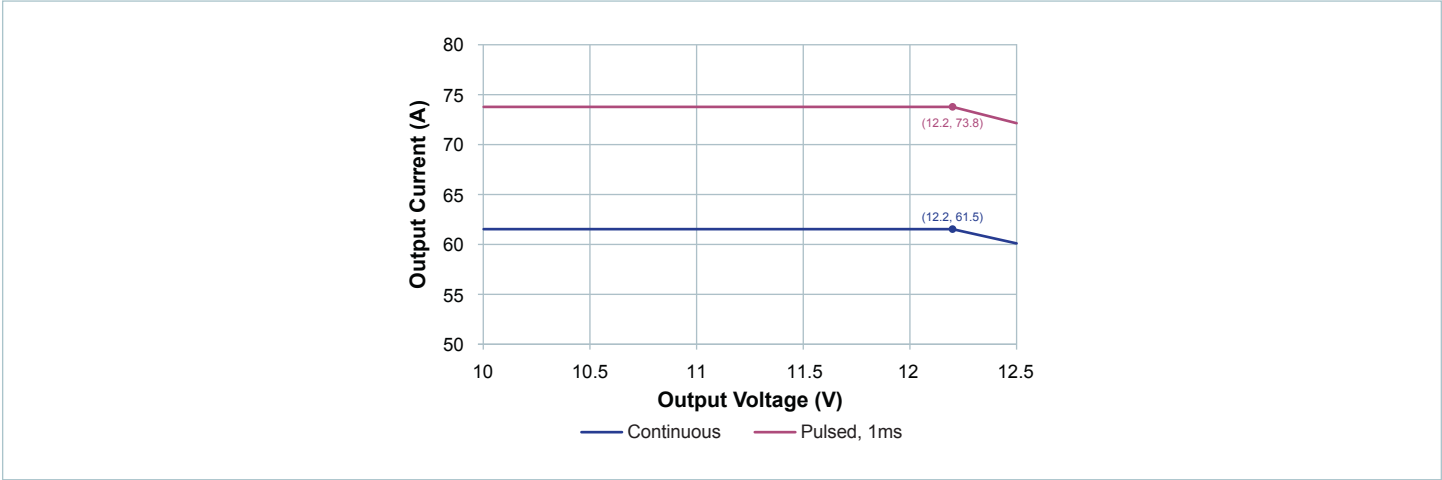


Figure 1 — Electrical specified operating area vs. output voltage, with thermal management to ensure  $T_{INT} < 125^{\circ}C$

Thermal Specified Operating Area

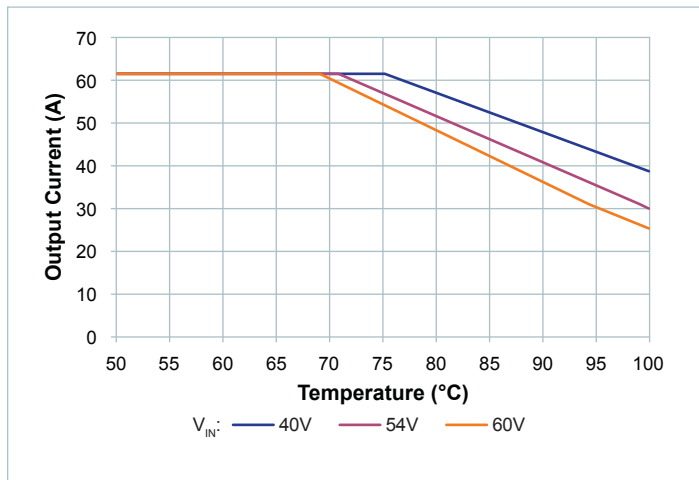


Figure 2 — Thermal specified operating area; top-side cooling, output current vs. case temperature,  $V_{OUT} = 10V$

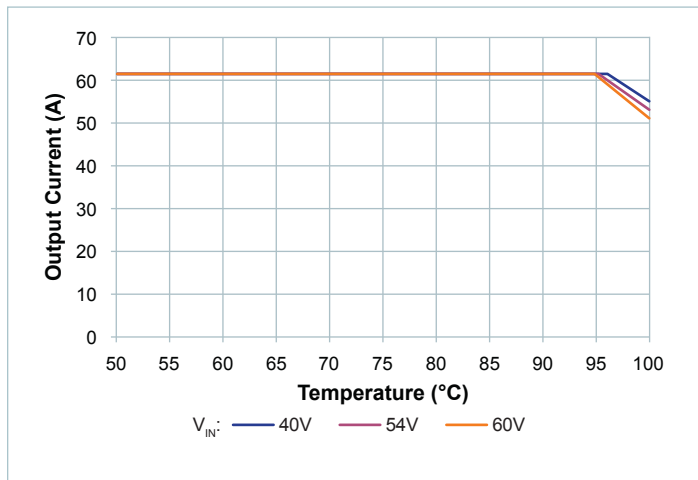


Figure 3 — Thermal specified operating area; double-sided cooling, output current vs. case temperature,  $V_{OUT} = 10V$

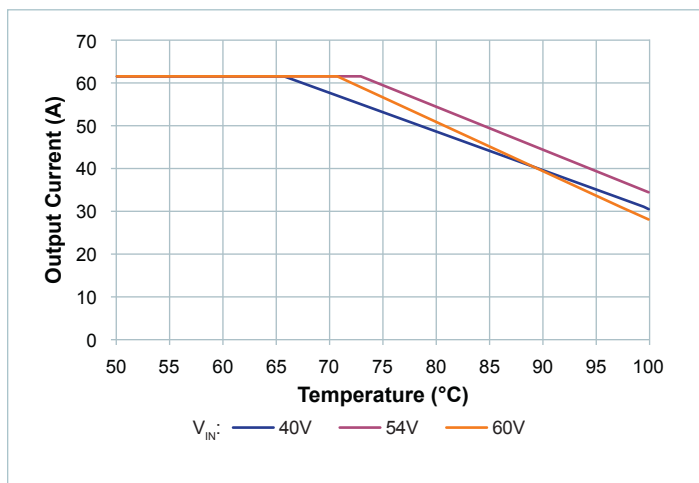


Figure 4 — Thermal specified operating area; top-side cooling, output current vs. case temperature,  $V_{OUT} = 12.2V$

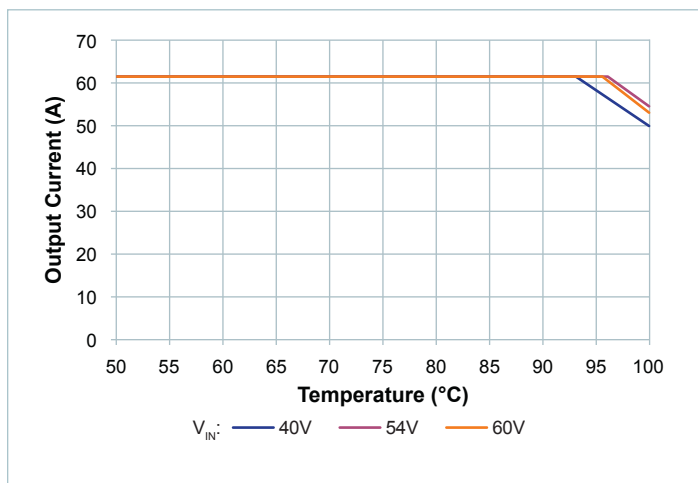


Figure 5 — Thermal specified operating area; double-sided cooling, output current vs. case temperature,  $V_{OUT} = 12.2V$

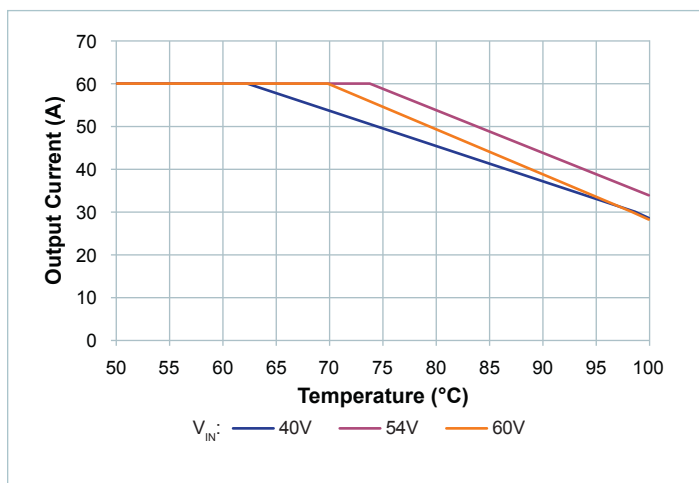


Figure 6 — Thermal specified operating area; top-side cooling, output current vs. case temperature,  $V_{OUT} = 12.5V$

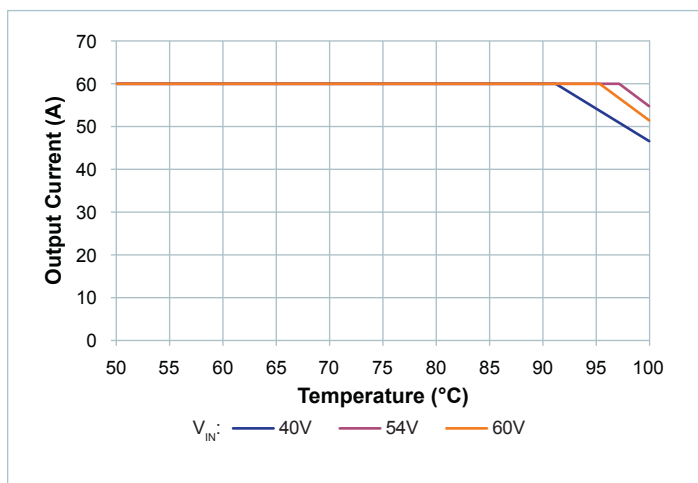


Figure 7 — Thermal specified operating area; double-sided cooling, output current vs. case temperature,  $V_{OUT} = 12.5V$

### Typical Performance Characteristics

The following figures present performance data in a typical application environment.

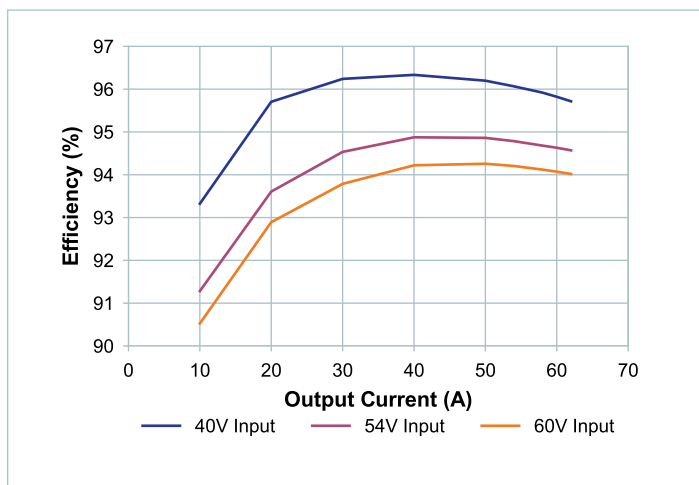


Figure 8 — Efficiency at 25°C case temperature,  $V_{OUT} = 10V$

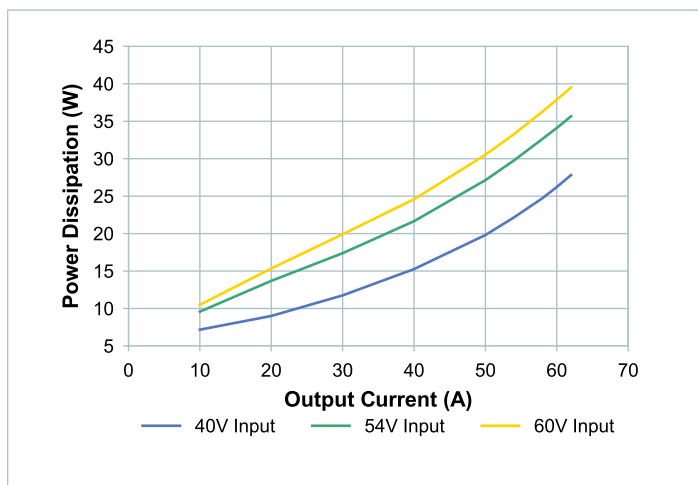


Figure 9 — Power dissipation at 25°C case temperature,  $V_{OUT} = 10V$

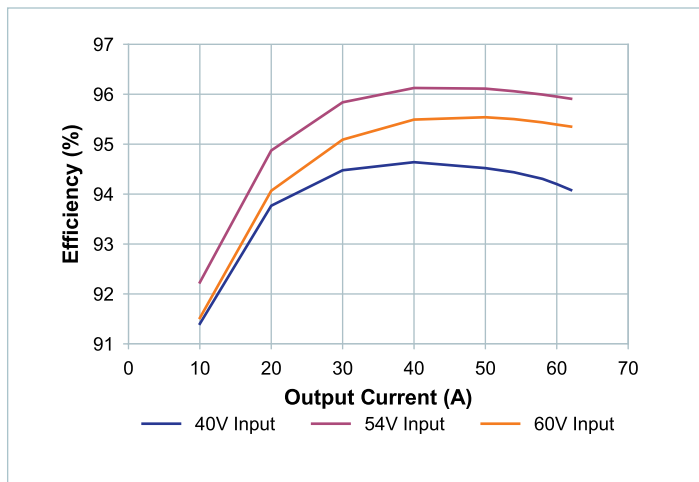


Figure 10 — Efficiency at 25°C case temperature,  $V_{OUT} = 12.2V$

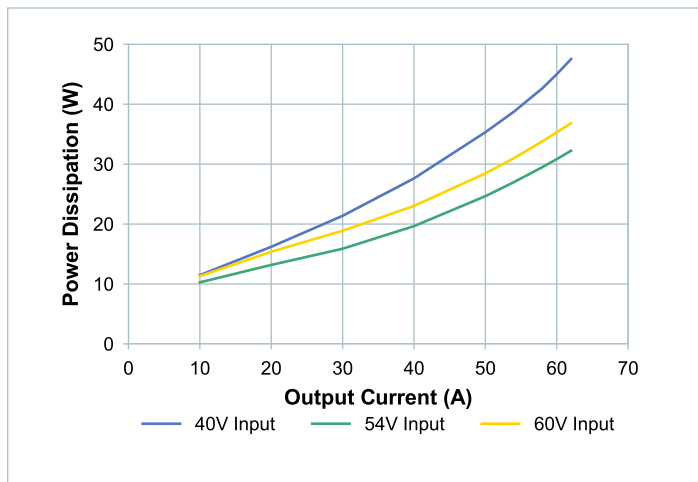


Figure 11 — Power dissipation at 25°C case temperature,  $V_{OUT} = 12.2V$

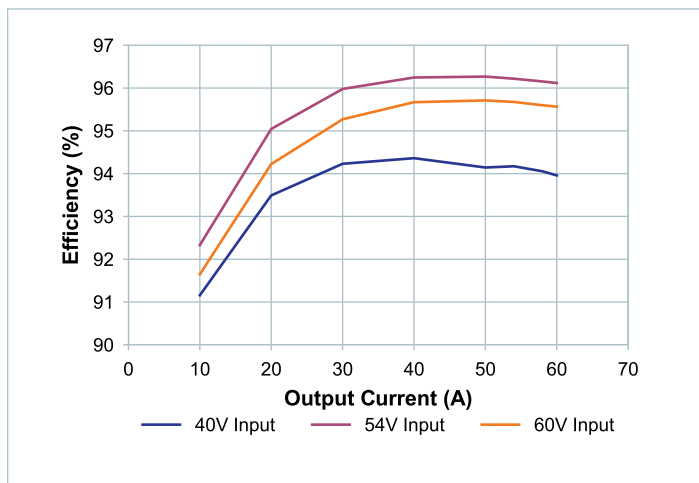


Figure 12 — Efficiency at 25°C case temperature,  $V_{OUT} = 12.5V$

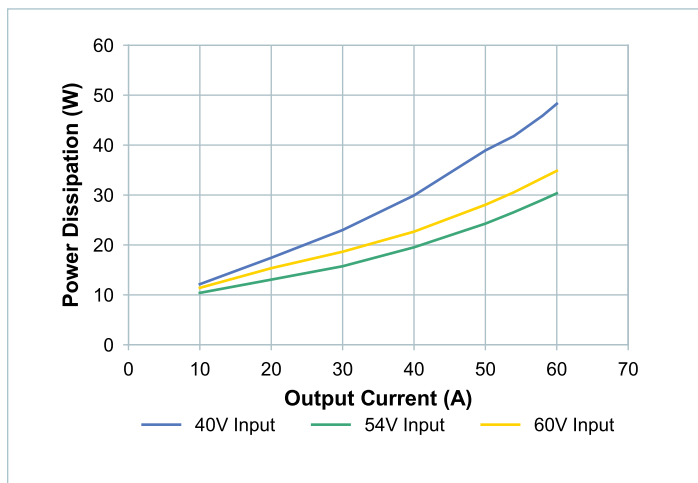


Figure 13 — Power dissipation at 25°C case temperature,  $V_{OUT} = 12.5V$

Typical Performance Characteristics (Cont.)

The following figures present performance data in a typical application environment.

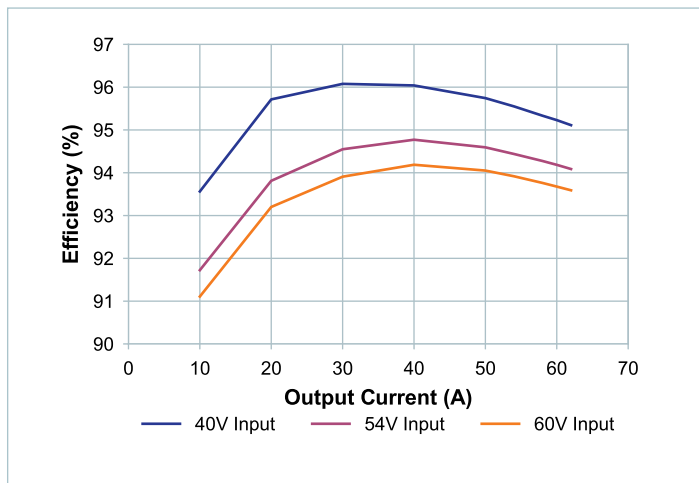


Figure 14 — Efficiency at 95°C case temperature,  $V_{OUT} = 10V$

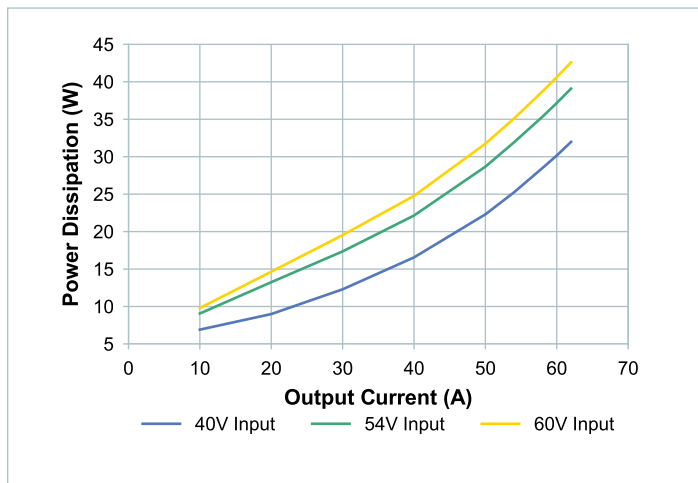


Figure 15 — Power dissipation at 95°C case temperature,  $V_{OUT} = 10V$

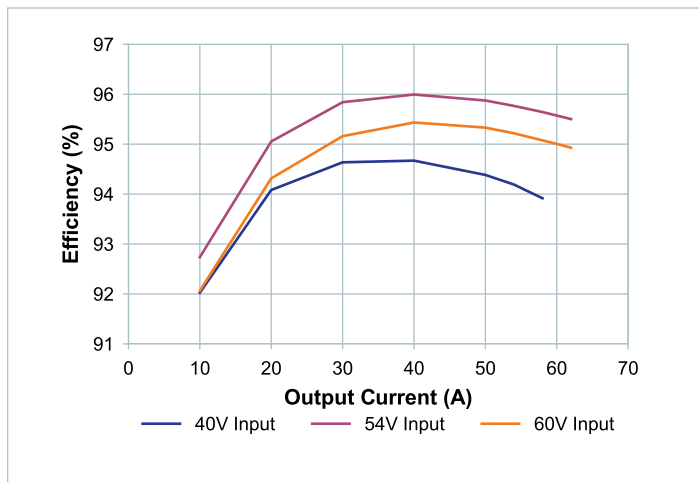


Figure 16 — Efficiency at 95°C case temperature,  $V_{OUT} = 12.2V$

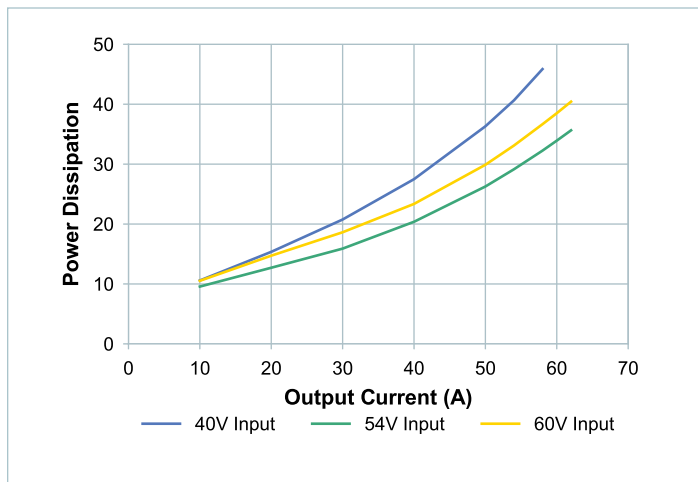


Figure 17 — Power dissipation at 95°C case temperature,  $V_{OUT} = 12.2V$

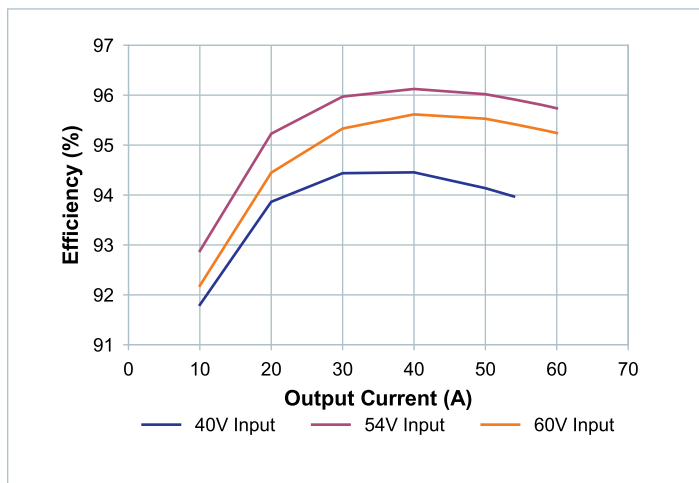


Figure 18 — Efficiency at 95°C case temperature,  $V_{OUT} = 12.5V$

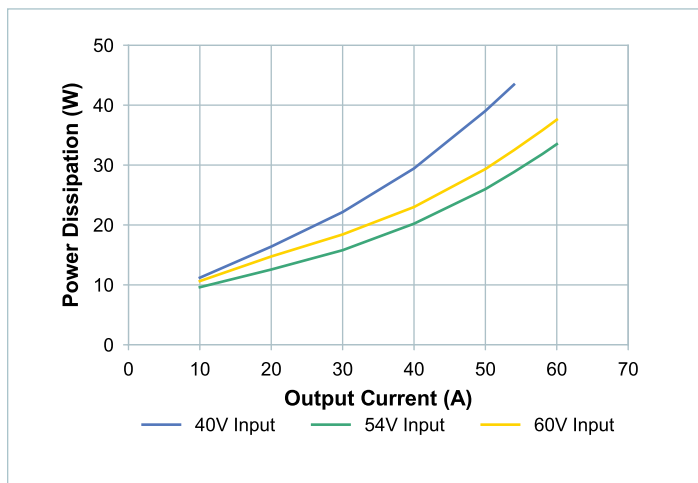


Figure 19 — Power dissipation at 95°C case temperature,  $V_{OUT} = 12.5V$

Typical Performance Characteristics (Cont.)

The following figures present performance data in a typical application environment.

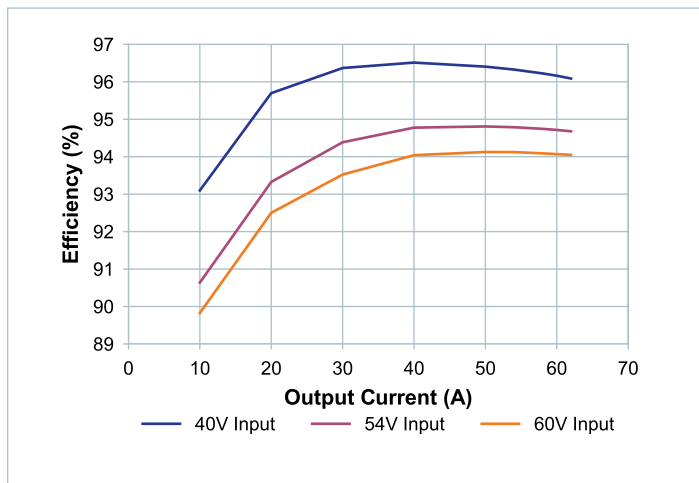


Figure 20 — Efficiency at  $-40^{\circ}\text{C}$  case temperature,  $V_{OUT} = 10\text{V}$

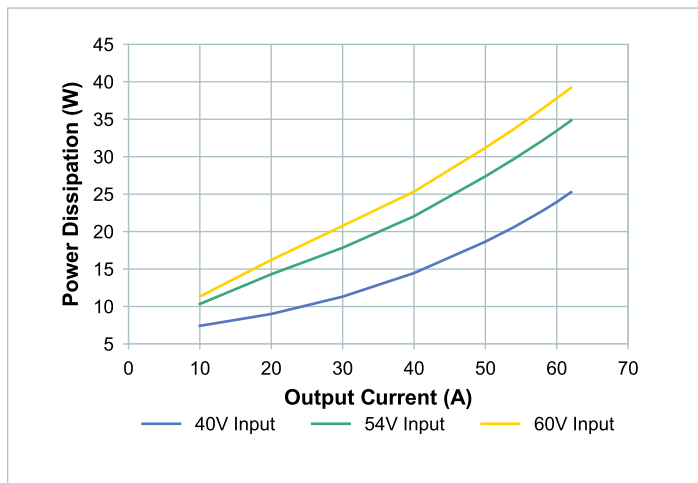


Figure 21 — Power dissipation at  $-40^{\circ}\text{C}$  case temperature,  $V_{OUT} = 10\text{V}$

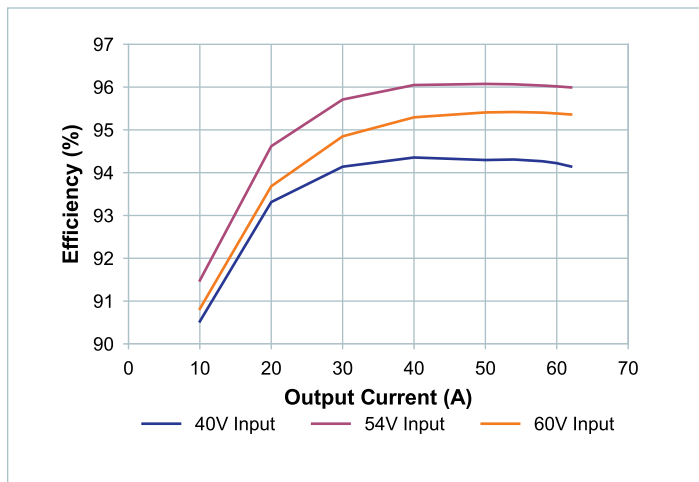


Figure 22 — Efficiency at  $-40^{\circ}\text{C}$  case temperature,  $V_{OUT} = 12.2\text{V}$

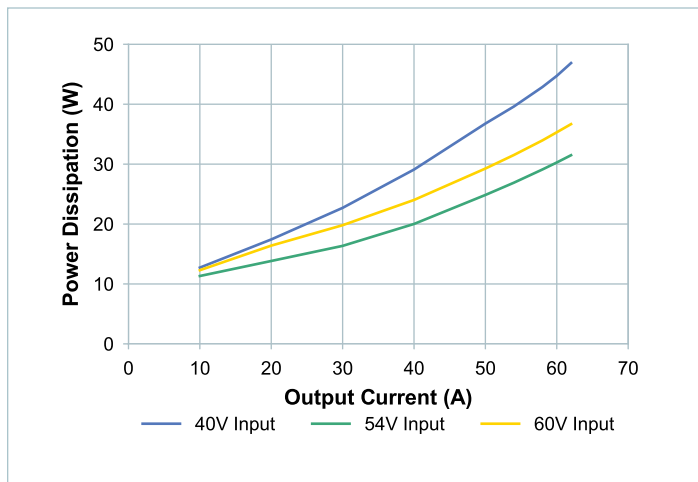


Figure 23 — Power dissipation at  $-40^{\circ}\text{C}$  case temperature,  $V_{OUT} = 12.2\text{V}$

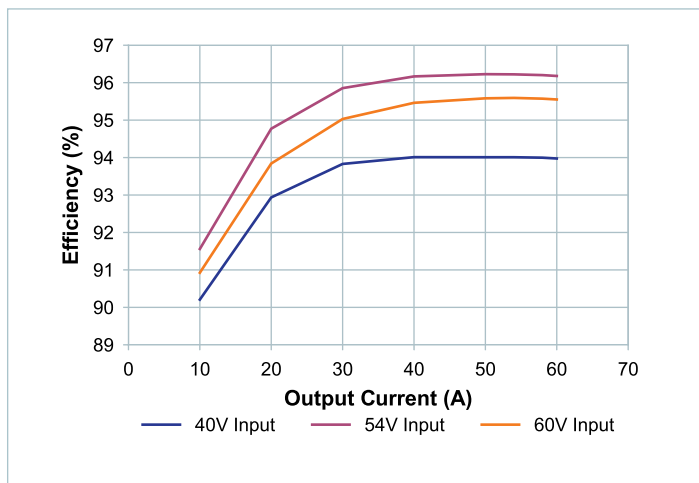


Figure 24 — Efficiency at  $-40^{\circ}\text{C}$  case temperature,  $V_{OUT} = 12.5\text{V}$

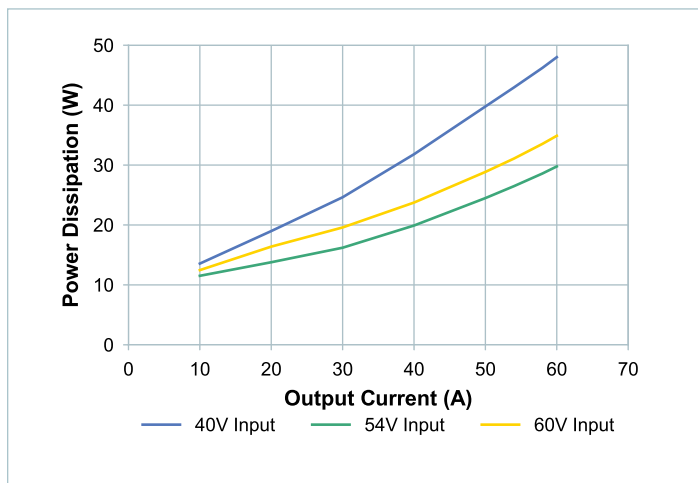


Figure 25 — Power dissipation at  $-40^{\circ}\text{C}$  case temperature,  $V_{OUT} = 12.5\text{V}$

## Terminal Descriptions

### **+IN – DCM Input Power**

The +IN terminal is the power input to the regulation stage. External filtering and decoupling techniques are application-specific. Low-ESR ceramic capacitors are recommended between the DCM input and power ground.

### **PGND – Power Ground**

The DCM is a three-terminal non-isolated regulator. PGND is the common power return for +IN and +OUT.

### **+OUT – DCM Output Power**

The +OUT terminal is the power output from the current multiplication stage. External filtering and decoupling techniques are application-specific. Low-ESR ceramic capacitors are recommended between the DCM output and power ground.

### **+INV – DCM Intermediate Power Node**

The +INV terminal is an intermediate power node between the regulation and current-multiplication powertrain stages.

### **EAO – Modulator Input**

The EAO terminal provides access to the error amplifier output and is the control node input to the regulation stage, which determines the DCM output power.

### **EN – Enable**

If the EN terminal is left floating or driven high, the DCM is enabled. When EN is pulled low, the DCM is disabled.

### **ADDR, SCL, SDA – PMBus Interface Address, Serial Clock and Serial Data**

Address is a multi-level analog input which sets the address at initial power-up. See PMBus® interface section for details on device address.

Serial clock (SCL) and serial data (SDA) require external pull-up resistors for normal operation. Refer to System Management Bus (SMBus) Specification version 3.0 for details.

### **$\overline{FLT}$ – Fault Monitor**

$\overline{FLT}$  is an open-drain terminal with an internal pull-up and indicates fault status.  $\overline{FLT}$  is active-low, so when any fault is active the terminal will drive low. When the module is enabled and not in a fault condition, the terminal will be pulled high. The module monitors the status of this terminal, so if an external sub-circuit pulls  $\overline{FLT}$  low, the module will also be disabled.

**Note:**  $\overline{FLT}$  displayed as FLT\* on the package drawing.

### **SYNCl – Factory Use Only**

Do not connect to the SYNCl terminal.

### **IMON – Factory Use Only**

Do not connect to the IMON terminal.

## Functional Description

The DCM is a non-isolated, regulated DC-DC power converter with PMBus® control and telemetry, in a thermally adept package. It consists of a ZVS buck-boost first-stage followed by a ZVS, ZCS Sine Amplitude Converter™ current multiplier second stage. The current multiplier operates at a fixed step-down ratio of 4, so all regulation is performed by Stage 1. The output voltage sense for the regulation control loop is taken at the module output terminals after the current multiplier, for tight regulation accuracy. All PMBus output voltage set-point control and telemetry is provided by Stage 1.

The DCM offers peak current and power ratings that are generally 20% higher than the continuous ratings for up to 1ms for dynamic loads and higher transient requirements. The full peak load capability is available up to an output voltage set point of 12.2V. Above 12.2V the peak current rating is linearly reduced to avoid risk of shut down due to an overvoltage event, as shown in Figure 1.

### DCM Power Up

When input voltage is applied, the DCM PMBus address is sensed and latched based on the pull-down resistor applied to the ADDR terminal. The address remains fixed until input voltage is removed.

### DCM Start Up

Any time the DCM input voltage is within  $V_{IN\_UVLO+}$  and  $V_{IN\_OVLO+}$ , the DCM has not been disabled via the EN or FLT control terminals, and it has recovered from any previously occurring faults, it will attempt to start.

At start up, the FLT terminal goes inactive (high) and the Stage 2 current multiplier begins switching. Then the Stage 1 buck-boost regulator begins switching and its reference rises to generate the soft-start ramp of the module's output voltage. The module output is capable of full rated continuous output current during soft-start.

The DCM output voltage rise is monotonic during soft start into static loads, once  $V_{OUT}$  exceeds 1.2V, provided the module has been disabled for at least  $t_{OFF-MONO}$ . If the module restarts more quickly than  $t_{OFF-MONO}$  then residual energy stored on the +INV node between the Stage 1 and Stage 2 powertrains can cause an output voltage transient to occur at the beginning of the soft-start ramp.

The DCM can start up into a precharged output up to 6.0V with no additional considerations. Starting the DCM into a precharged  $V_{OUT}$  higher than 6.0V is not recommended due to the risk that ring-up could trigger a  $V_{OUT-OVP}$  fault.

### Pulse-Skip Mode (PSM)

The ZVS buck-boost stage features a hysteretic pulse-skipping mode. At light-load conditions, switching cycles can be skipped in order to significantly reduce gate-drive power and improve efficiency. The regulator will automatically enter and exit PSM based on load. Depending on line and trim operating conditions, as well as capacitor and other component values, PSM may result in occasional skipping of one or many switching cycles.

## Variable-Frequency Operation

The ZVS buck-boost stage is pre-programmed to a fixed, maximum base operating frequency. The maximum processed power determines the base frequency and associated power inductor with respect to other constraints to achieve peak efficiency at nominal operation. The operating frequency can be reduced from the base frequency as needed to maintain rated power capability at certain line voltage, trim voltage and load conditions. By reducing the operating frequency, or stretching the period of each switching cycle, the ZVS operation is preserved throughout the input line voltage range maintaining optimum efficiency. The current-multiplication stage also exhibits variable-frequency operation, though over a smaller frequency range relative to that of the ZVS buck-boost stage.

### DCM Fault Response

If the DCM detects a fault condition, the FLT terminal drives low and the module stops processing power within the fault detection response time  $t_{FAULT}$ . The input overvoltage, input undervoltage, and overtemperature fault conditions, as well as FLT terminal low are continuously monitored, and the DCM will not restart as long as they persist. Once the fault condition is removed and the appropriate fault recovery time ( $t_{FAULT1\_RECOVERY}$  or  $t_{FAULT2\_RECOVERY}$ ) has elapsed, the DCM will release FLT and will attempt a restart. Other fault types like overload or short circuit condition can only occur when the module is operating. After shut down, the DCM will repeatedly attempt a restart after a delay, and will shut down again as long as the load fault condition persists.

### Input Undervoltage Recovery and Lockout Thresholds ( $V_{IN\_UVLO+}$ and $V_{IN\_UVLO\_HYS}$ )

The regulator stage monitors the +IN terminal. The DCM will not start until the input voltage exceeds the undervoltage recovery threshold ( $V_{IN\_UVLO+}$ ) and will shut down if the input voltage crosses below this threshold by more than the undervoltage lockout hysteresis ( $V_{IN\_UVLO\_HYS}$ ).

A  $V_{IN\_UVLO}$  will set byte 0, bit 3 in the MFR\_STATUS\_FAULTS (F0h) status register, as well as byte 1, bit 0 FLT\_FALLING\_EDGE.

### Input Overvoltage Lockout and Recovery Thresholds ( $V_{IN\_OVLO+}$ and $V_{IN\_OVLO\_HYS}$ )

If the input voltage rises above the overvoltage lockout threshold ( $V_{IN\_OVLO+}$ ), the DCM will shut down. The DCM will attempt to recover once the input voltage has decreased below this threshold by at least the overvoltage lockout hysteresis ( $V_{IN\_OVLO\_HYS}$ ).

A  $V_{IN\_OVLO}$  will set byte 0, bit 4 in the MFR\_STATUS\_FAULTS (F0h) status register, as well as byte 1, bit 0 FLT\_FALLING\_EDGE.

### Overtemperature Fault Threshold ( $T_{OT}$ )

The DCM features an overtemperature shut down, which is designed to protect against catastrophic failure due to excessive temperatures. The overtemperature shut down cannot be used to ensure the device stays within the recommended operating temperature range, because when the overtemperature threshold  $T_{OT}$  engages,  $T_{INT}$  is at or above the maximum rated temperature of 125°C. When an overtemperature shut down occurs, the DCM stops processing power and  $\overline{FLT}$  drives low. The DCM will restart after the temperature has decreased below  $T_{OT}$  by at least the overtemperature restart hysteresis,  $T_{OT\_HYS}$ .

If the overtemperature fault threshold is exceeded, byte 2, bit 0 in the MFR\_STATUS\_FAULTS (F0h) status register will be set. Unlike other faults, the Overtemperature Fault will not set byte 1, bit 0 FLT\_FALLING\_EDGE due to how the overtemperature condition is sensed.

### $\overline{FLT}$ Fault

If the  $\overline{FLT}$  terminal is pulled low, the unit will shut down in the same manner as other faults listed here. Byte 1, bit 0 FLT\_FALLING\_EDGE bit will be set in the MFR\_STATUS\_FAULTS (F0h) status register.

### Output Voltage Negative ( $V_{OUT\_NEG}$ )

When the DCM output voltage is higher than  $V_{OUT\_NEG\_RE-ARM}$ , the Output Voltage Negative fault is armed. Once armed, if the DCM output voltage becomes reverse-biased by more than  $V_{OUT\_NEG}$ , it will shut down and stop processing power. It will also set byte 0, bit 6 in the MFR\_STATUS\_FAULTS (F0h) status register, as well as byte 1, bit 0 FLT\_FALLING\_EDGE.

This can occur if the module is disabled or shuts down due to another fault or if the load is inductive and brings  $V_{OUT}$  below ground.

When the DCM is disabled via EN, or has shut down due to any fault type, the Output Voltage Negative fault is blanked from further activation until the output voltage again exceeds  $V_{OUT\_NEG\_RE-ARM}$ . This permits the DCM to be easily restarted even when a negative  $V_{OUT}$  condition persists (as may be the case if a downstream current sink is present).

### Output Overvoltage Threshold ( $V_{OUT\_OVP}$ )

The DCM will shut down if the voltage at +INV rises above the OVP threshold,  $V_{OUT\_OVP}$ . The sense point is taken before the second-stage current multiplier, so the effective output-referred threshold depends on the voltage drop across the second stage. The DCM will restart after the recovery time  $t_{FAULT2\_RECOVERY}$ .

A  $V_{OUT\_OVP}$  fault can also be produced by the ZVS buck-boost stage. If the buck-boost produces the OVP event, the DCM will restart after the recovery time  $t_{FAULT1\_RECOVERY}$ .

A  $V_{OUT\_OVP}$  fault will set byte 0, bit 5 in the MFR\_STATUS\_FAULTS (F0h) status register, as well as byte 1, bit 0 FLT\_FALLING\_EDGE.

### Output OVP Relative ( $\%_{EAIN\_HI}$ )

The DCM will shut down if the module output voltage is more than  $\%_{EAIN\_HI}$  higher than the programmed output voltage, for more than  $t_{EAIN\_HI}$ . This fault detection is inactive during soft start as well as for timeout period  $t_{EAIN\_HI}$  following a  $V_{OUT\_COMMAND}$  change to output voltage trim.

$\%_{EAIN\_HI}$  will set EAIN\_HI, byte 1, bit 5 in the MFR\_STATUS\_FAULTS (F0h) status register, as well as byte 1, bit 0 FLT\_FALLING\_EDGE.

**Note:** at higher output voltage set points, the fault may be reported as  $V_{OUT\_OVP}$ .

### EAO Overload ( $V_{EAO\_OL}$ )

EAO is the control input to the Stage 1 regulator. The EAO voltage is driven by the internal transconductance error amplifier closing the voltage control loop. The voltage on EAO can exceed the EAO Overload Threshold voltage ( $V_{EAO\_OL}$ ) when the DCM is overloaded.

A timer permits transient overload conditions to occur without triggering the fault detection. However if EAO remains above its overload threshold for longer than  $t_{EAO\_OL}$ , the DCM will shut down and  $\overline{FLT}$  will be driven low.

The EAO Overload fault will set byte 1, bit 1 in the MFR\_STATUS\_FAULTS (F0h) status register, as well as byte 1, bit 0 FLT\_FALLING\_EDGE.

### Overcurrent Threshold ( $I_{OC}$ )

The DCM output current is continuously measured during operation, and if it exceeds the overcurrent shut-down threshold ( $I_{OC}$ ), for longer than overcurrent timeout ( $t_{IOC}$ ), the DCM will shut down and  $\overline{FLT}$  is driven low. The overcurrent is monitored by both the current multiplier stage and the buck-boost regulation stage. If the buck-boost stage detects the overcurrent ( $I_{OC1}$ ), then the MFR\_STATUS\_FAULTS bits  $V_{OUT\_NEG}$  or  $Q3\_SIL$  may set. If only the current multiplier stage detects the fault ( $I_{OC2}$ ), then only the  $\overline{FLT}$  terminal falling edge will be set. Any of these bits indicate the presence of an overcurrent condition. The DCM will restart after the recovery time  $t_{FAULT1\_RECOVERY}$  or  $t_{FAULT2\_RECOVERY}$  depending on which powertrain stage shut down.

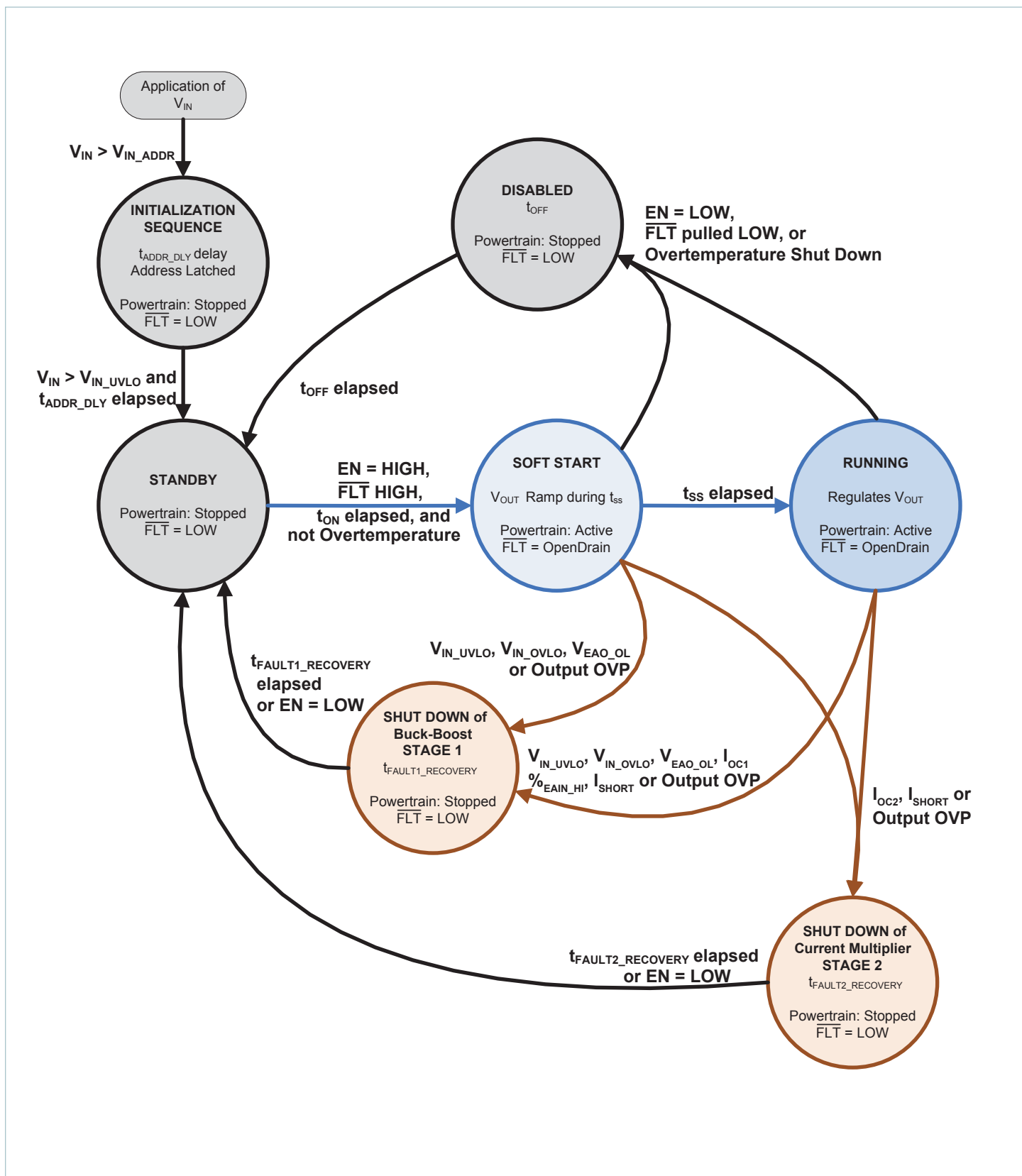
### Short Circuit Detection ( $I_{SHORT}$ )

In the event of a short circuit occurring during operation or during start up, the DCM fast short-circuit detection will shut down the powertrain and drive  $\overline{FLT}$  low. The MFR\_STATUS\_FAULTS bits  $Q1\_FIL$  or  $Q3\_FIL$  should set. The  $V_{OUT\_NEG}$  may also set. The DCM will restart after the recovery time  $t_{FAULT1\_RECOVERY}$  or  $t_{FAULT2\_RECOVERY}$ , depending on which powertrain stage shut down. For the case where the short-circuit condition occurs while the DCM is running, the  $\overline{FLT}$  line will be asserted after  $t_{FAULT}$ . For start up into a short-circuit condition or during the restart after  $t_{FAULT1\_RECOVERY}$  while a short is still applied, there is a delay of ~3ms from powertrain shut down to the activation of  $\overline{FLT}$ .



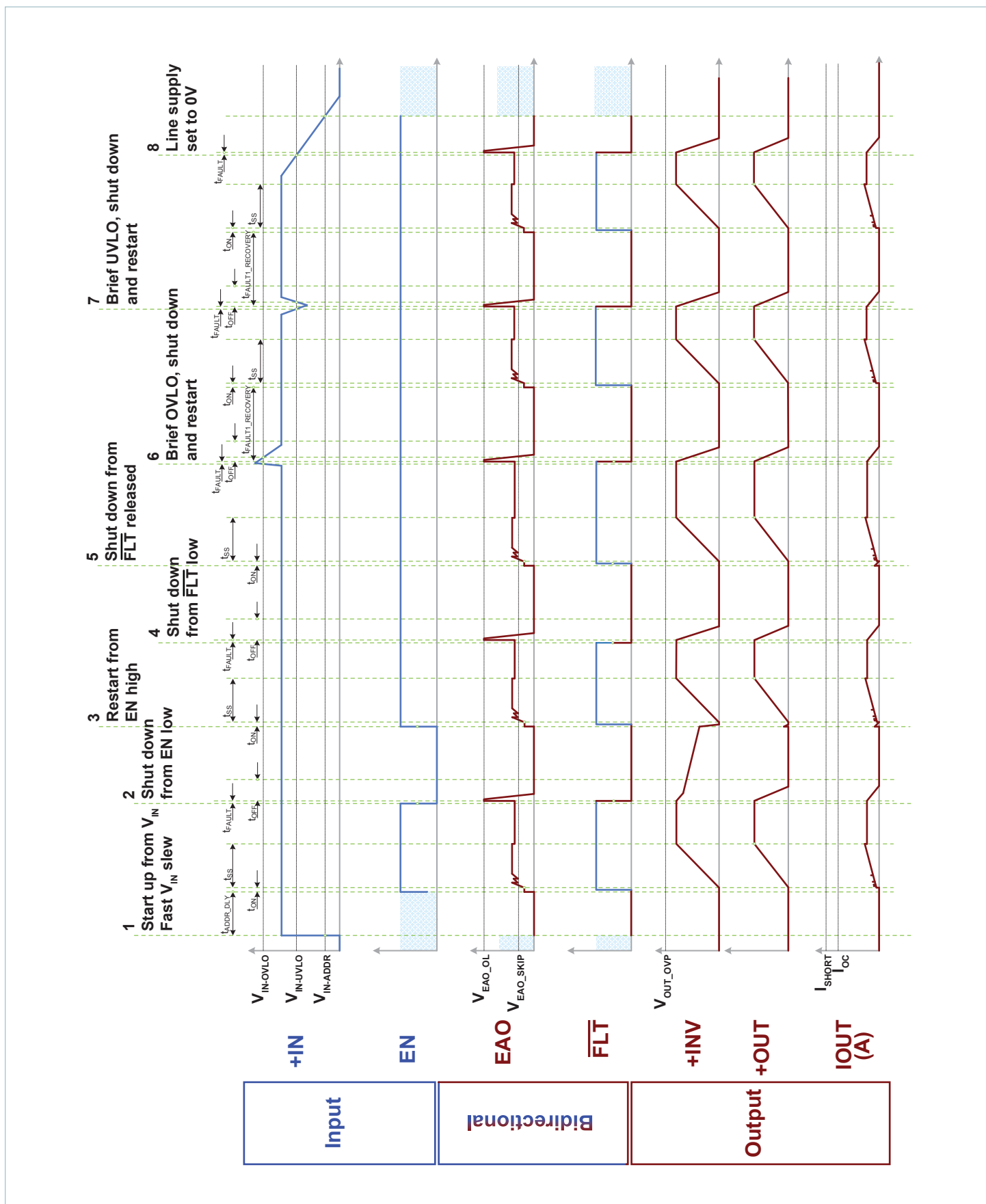
### High-Level Functional State Diagram

Conditions that cause state transitions are shown along arrows. Sub-sequence activities listed inside the state bubbles.



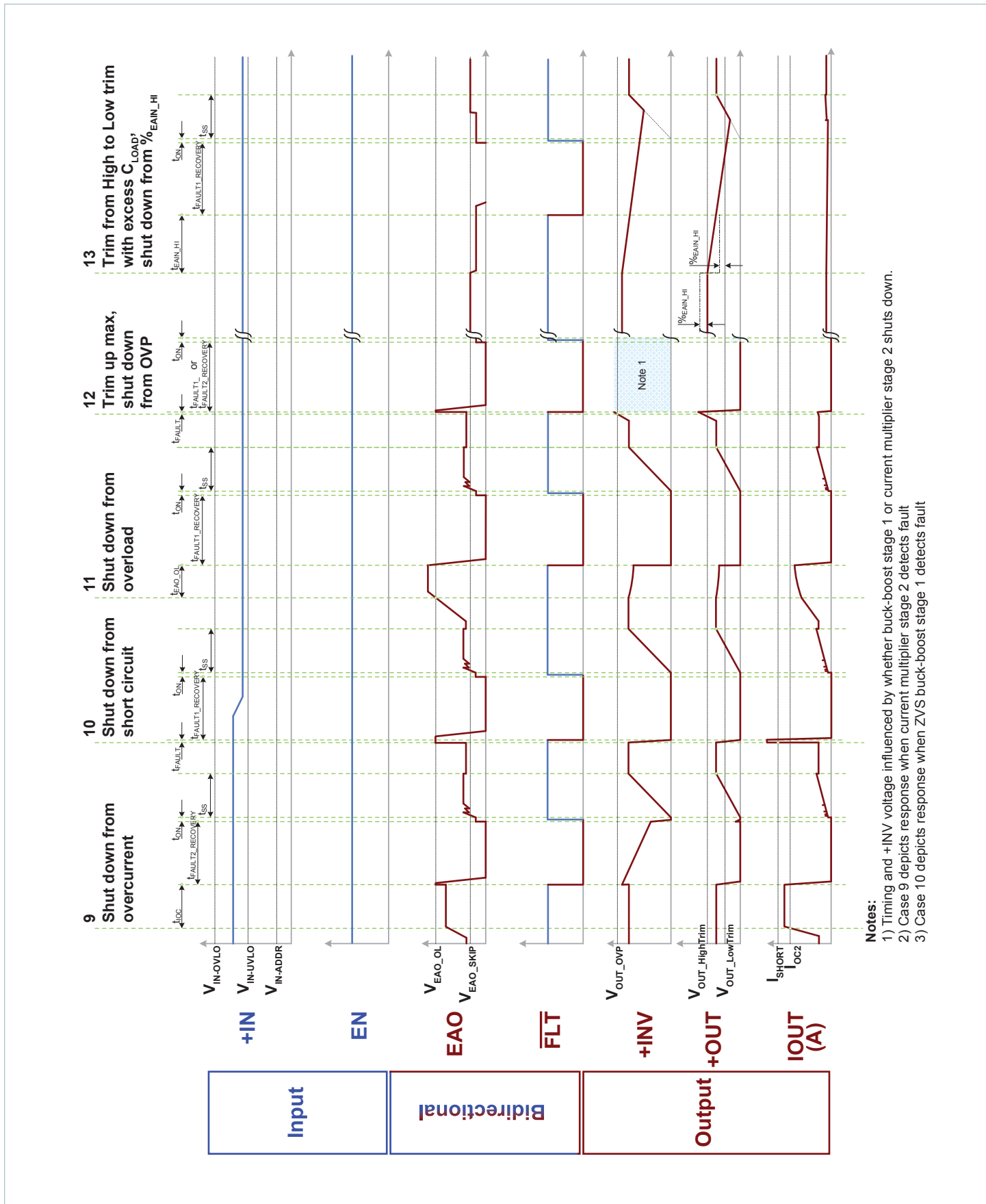
Timing Diagrams

Module inputs are shown in blue; module outputs are shown in brown.



Timing Diagrams (Cont.)

Module inputs are shown in blue; module outputs are shown in brown.



**Notes:**  
 1) Timing and +INV voltage influenced by whether buck-boost stage 1 or current multiplier stage 2 shuts down.  
 2) Case 9 depicts response when current multiplier stage 2 detects fault  
 3) Case 10 depicts response when ZVS buck-boost stage 1 detects fault

## Design Guidelines

### Input Filter Stability

Regulating switch-mode power supplies like the DCM present a negative impedance to the voltage source that is powering them. To ensure stability of the regulation loop, the source impedance and the parasitic resistance and inductance of the interconnect lines must be considered. The high performance ceramic decoupling capacitors placed locally to the input of the DCM are effective in controlling reflected ripple current at the switching frequency. However their low ESR means they will not significantly dampen an excessively high impedance of an upstream voltage source.

The worst-case minimum regulator dynamic input impedance magnitude  $|r_{EQ\_IN}|$  can be calculated by dividing the lowest line voltage by the full load input current. To ensure stability, two cases must be considered.

#### *Input Filter case 1; inductive source and local, external, input decoupling capacitance with negligible ESR (i.e., ceramic type)*

The voltage source impedance can be modeled as a series  $R_{LINE}$   $L_{LINE}$  circuit. In order to guarantee stability the following conditions

$$R_{LINE} > \frac{L_{LINE}}{(C_{IN} + C_{IN\_EXT}) \cdot |r_{EQ\_IN}|} \quad (1)$$

$$R_{LINE} \ll |r_{EQ\_IN}| \quad (2)$$

must be verified:

Notice that the local high-performance ceramic input capacitors should be included for this purpose. Equation 2 means that the line source impedance should be <10% of the regulator's dynamic input resistance  $r_{EQ\_IN}$  for best performance. The line source impedance, however, must be <50% of  $r_{EQ\_IN}$ . Note that  $R_{LINE}$  cannot be made arbitrarily low otherwise Equation 1 is violated and the system will show instability, due to under-damped RLC input network.

#### *Input Filter case 2; inductive source and internal, external input decoupling capacitance with significant $R_{C_{IN\_EXT}}$ ESR (i.e., electrolytic type)*

In order to simplify the analysis in this case, the input source impedance can be modeled as a simple inductor  $L_{LINE}$ . Notice that, the internal high-performance ceramic capacitors  $C_{IN}$  directly at the input of the DCM should be included in the external electrolytic capacitance value for this purpose. The stability criteria will be:

$$|r_{EQ\_IN}| > R_{C_{IN\_EXT}} \quad (3)$$

$$\frac{L_{LINE}}{(C_{IN\_EXT} \cdot R_{C_{IN\_EXT}})} < |r_{EQ\_IN}| \quad (4)$$

Equation 4 shows that if the aggregate ESR is too small – for example by using only high-Q ceramic input capacitors ( $C_{IN\_EXT}$ ) – the system will be under-damped and may not be stable. As with Equation 2 above, a decade of margin in satisfying Equation 3 is preferred, but an octave of margin is considered the minimum.

Additional information can be found in the filter design application note [AN:023](#). Lastly, consider the DCM maximum input voltage slew rate  $dV_{IN}/dt$ , which is needed to prevent overstress to input stage components in the module. Additional circuitry may be required at the DCM input if the filter solution can exceed that slew rate.

### Input Fuse Recommendations

A fuse should be incorporated at the input to the DCM, in series with the +IN terminal. A 30A or smaller input fuse (Littelfuse® Nano<sup>2</sup>® 456 Series) is required to comply with safety agency conditions of acceptability. Always ascertain and observe the safety, regulatory, or other agency specifications that apply to your specific application.

**Thermal Design**

Thermal management of DCM internal power dissipation is critical to reliable operation, and ample cooling is preferred since efficiency and reliability are better at lower internal temperatures. Figure 26 shows a thermal impedance model that can estimate the maximum temperature of the highest temperature component for a given electrical and thermal operating condition.

The circuit model assumes each of those areas identified as thermal boundaries is isothermal, although not necessarily the same temperature as the other boundary areas. Use of electrically insulating thermal interface material is required to prevent shorting conductive surfaces on the DCM case.

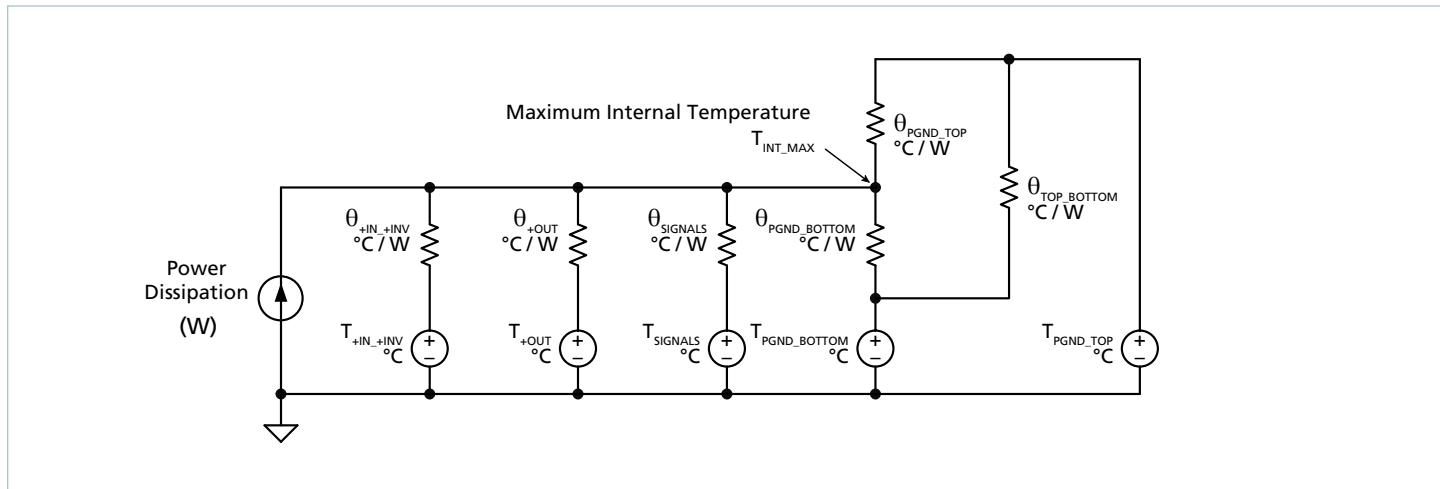


Figure 26 — Thermal model

Symbol	Thermal Impedance (°C / W)	Definition of Estimated Thermal Resistance
$\theta_{PGND\_TOP}$	1.4	from the hottest component inside the DCM to the circuit board it is mounted on at PGND_TOP
$\theta_{+IN\_+INV}$	23	from the hottest component inside the DCM to the circuit board it is mounted on at +IN_+INV
$\theta_{+OUT}$	15	from the hottest component inside the DCM to the circuit board it is mounted on at +OUT
$\theta_{SIGNALS}$	18	from the hottest component inside the DCM to the circuit board it is mounted on at SIGNALS
$\theta_{PGND\_BOTTOM}$	1.7	from the hottest component inside the DCM to the circuit board it is mounted on at PGND_BOTTOM
$\theta_{TOP\_BOTTOM}$	10	from PGND_TOP to PGND_BOTTOM

Table 1 — Thermal impedance

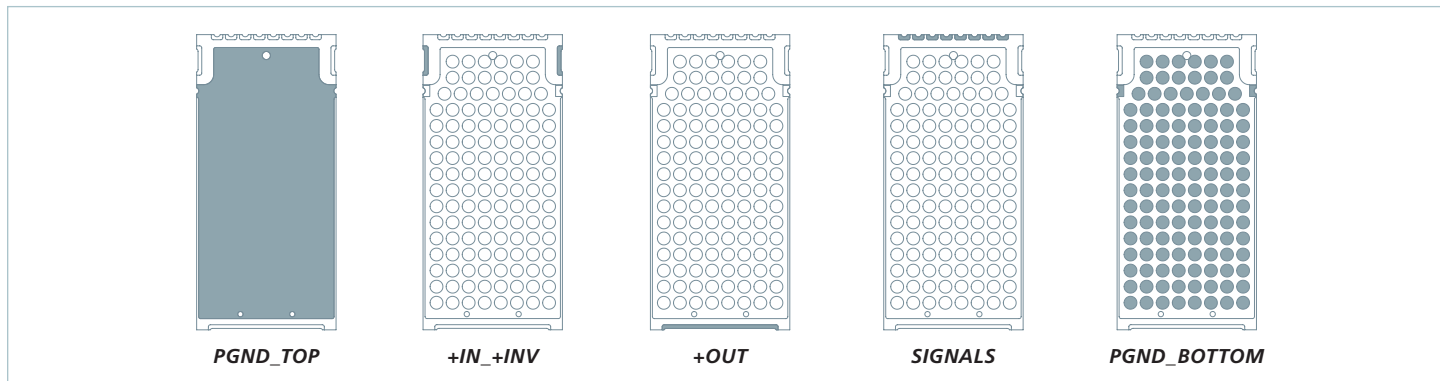


Figure 27 — Thermal model boundary conditions; area defined as shaded

Thermal Design — Typical Performance

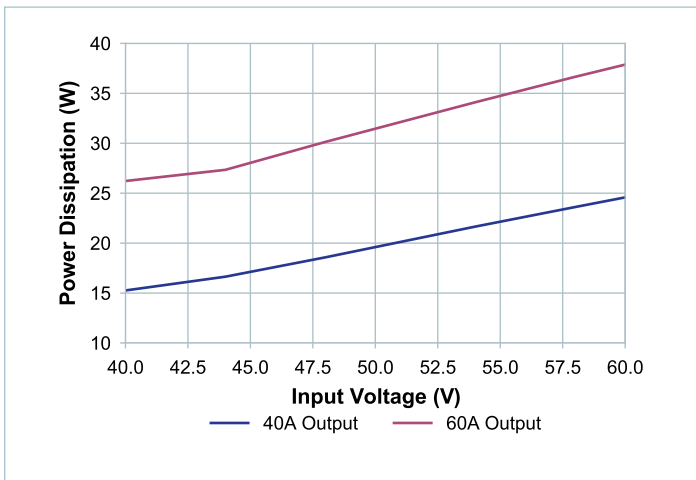


Figure 28 — Power dissipation vs. line voltage,  $V_{OUT} = 10V$ , at 25°C case temperature

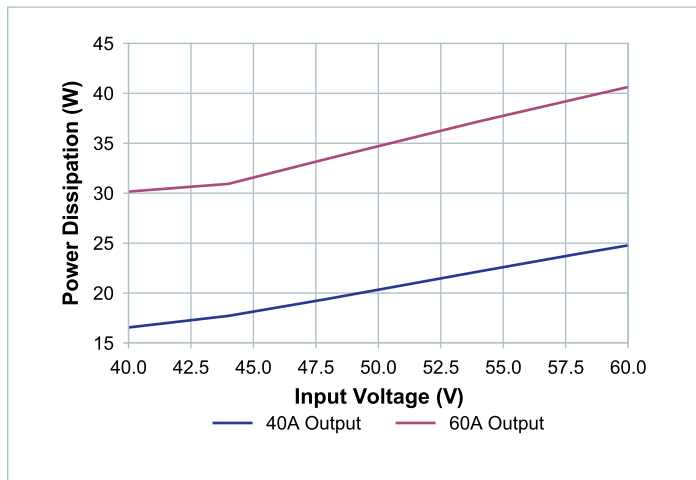


Figure 29 — Power dissipation vs. line voltage,  $V_{OUT} = 10V$ , at 95°C case temperature

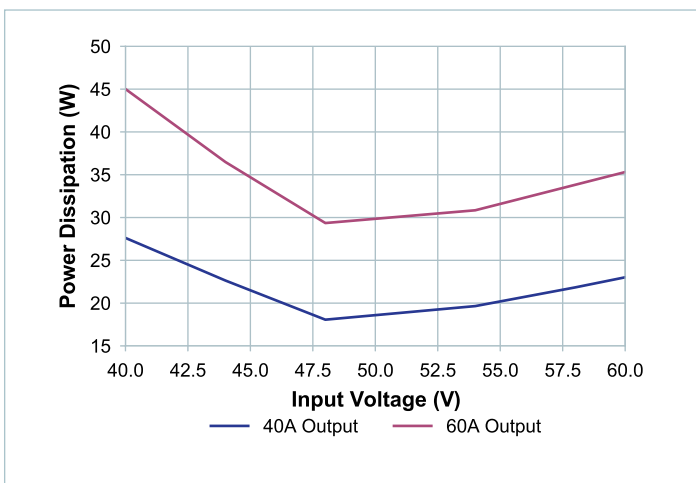


Figure 30 — Power dissipation vs. line voltage,  $V_{OUT} = 12.2V$ , at 25°C case temperature

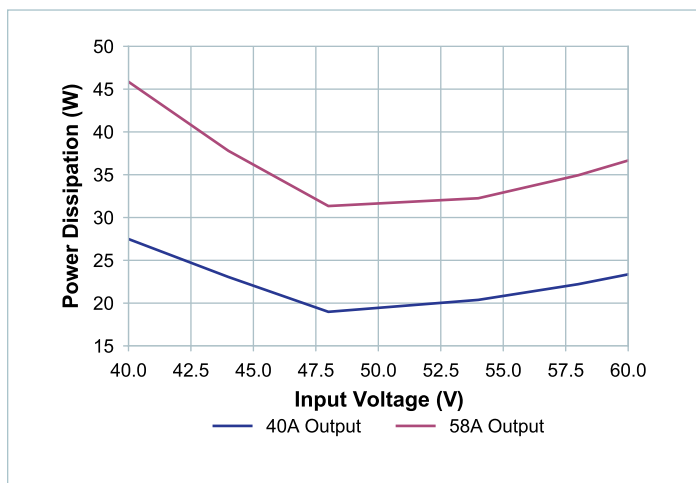


Figure 31 — Power dissipation vs. line voltage,  $V_{OUT} = 12.2V$ , at 95°C case temperature

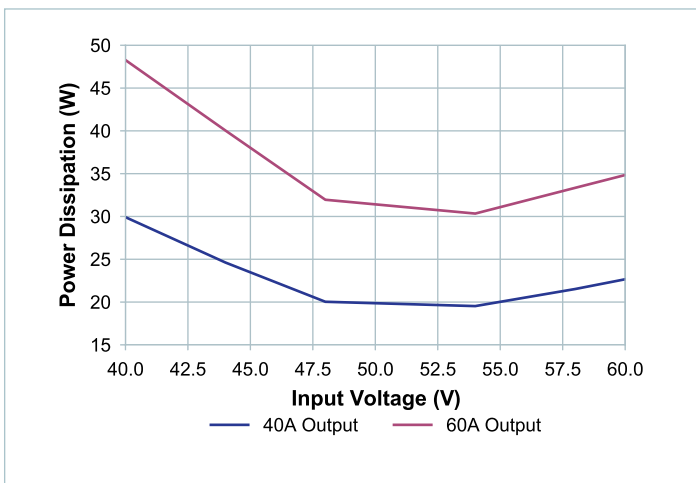


Figure 32 — Power dissipation vs. line voltage,  $V_{OUT} = 12.5V$ , at 25°C case temperature

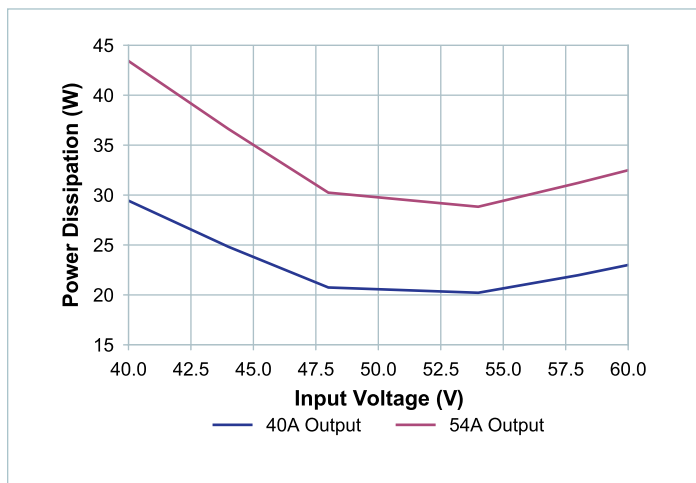
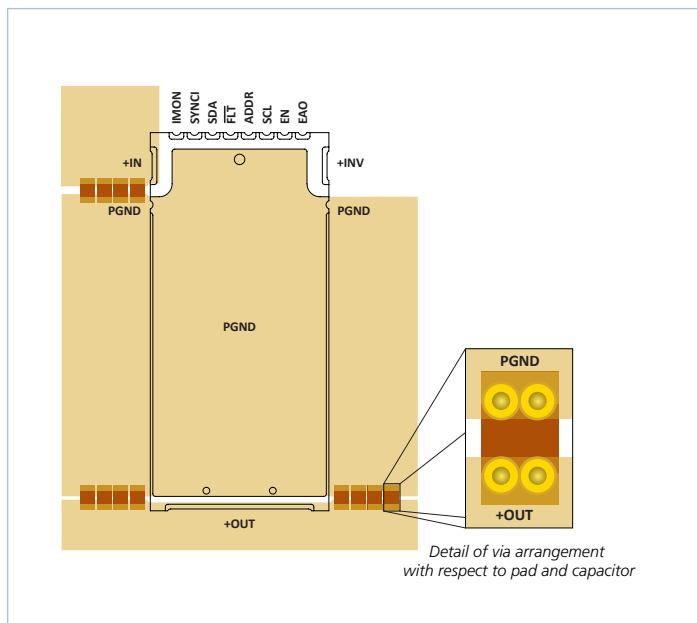


Figure 33 — Power dissipation vs. line voltage,  $V_{OUT} = 12.5V$ , at 95°C case temperature

### Additional PCB Layout Considerations

DCM output capacitance is needed to bypass the high-frequency ripple at its source. The amount of capacitance varies by design and should be distributed as shown in the diagram.

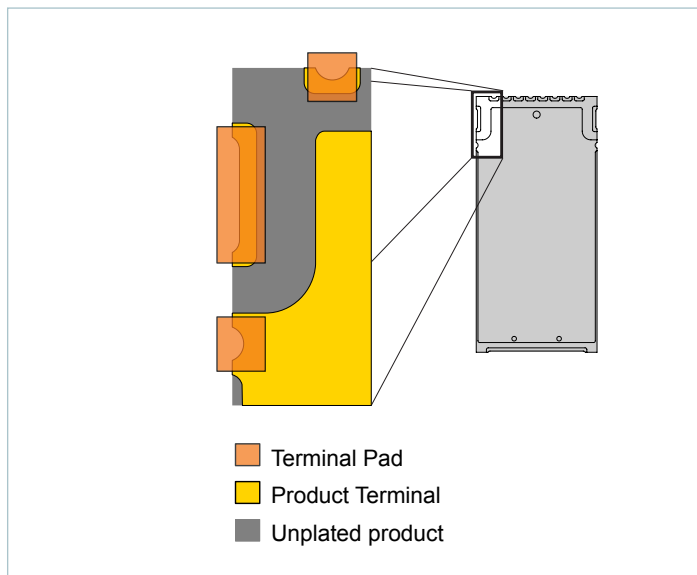


**Figure 34** — Recommended positioning of external capacitance relative to +IN, +OUT and PGND terminals

The mechanical drawings in later sections include the recommended land pattern to use when creating a PCB footprint. The recommend footprint pad is intentionally narrower than the actual product terminal. This allows room for the pick-and-place machine worst-case placement tolerances. The worst case is a package terminal exactly aligned with the inner edges of footprint pad.

If the product is water washed post assembly, then the PGND circular thermal pads under the product must be copper-defined.

If no-clean solder flux is used during assembly, then PGND thermal pad apertures may be solder-mask-defined.



**Figure 35** — Product drawing vs. recommended land pattern

### Parallel Operation for High Power Arrays

Loads that exceed the rated current or power of a single DCM can be powered by an array of DCMs, with array sizes up to  $n_{\text{ARRAY max}}$  modules. A properly configured array of  $n$  DCMs provides the rated power or current of a single module times  $n$ , with no electrical de-rating required.

At the schematic level, a DCM array is configured by setting a unique address for each DCM and directly interconnecting the control terminals: EN, FLT, SDA and SCL. Additionally, all EAO terminals must be interconnected.

For power connections in an array, each DCM should still have dedicated multi-layer chip capacitors at the input and output. The DCM +OUT terminals must be directly connected together. The DCM +IN terminals are not directly connected, but instead each has its own dedicated fuse and input filter. The fuse and filter of each DCM in the array must be powered from the same voltage source; different input voltages are not permitted.

PCB layout for an array of DCMs builds off of the recommended layout shown in Figure 34. The DCMs should be placed in close proximity so that interconnected control signals can be short, which reduces stray capacitance and pickup of noise. However DCMs must still be separated sufficiently to permit adequate cooling to avoid excess internal temperatures. If the PCB provides the dominant cooling path for heat to flow from the modules, physical separation of modules becomes more important. PGND should be carried on contiguous plane layers to optimize effectiveness of high-frequency bypassing and filtering. The +OUT connection should also be on plane layers to minimize inductance between DCM outputs. Control signal route lengths should be minimized but they should not be routed underneath the DCM body. This is especially true for EAO.

## PMBus Interface

Refer to “PMBus Power System Management Protocol Specification Revision 1.3, Parts I and II.” For complete PMBus® specifications details visit <http://pmbus.org>

The DCM is a PMBus child and will respond only to host commands listed in this section. Dedicated address (ADDR), clock (SCL) and data (SDA) terminals are available; the optional SMBALERT# signal is not supported.

### Device Address

The DCM PMBus address can be set using a 1% resistor from the ADDR terminal to ground. The following table lists the available addresses and the corresponding resistor value to use.

The DCM does not support SMBus Address Resolution protocol. The address is set at initial power up and then remains fixed until power is removed.

7-bit Hex Address	Resistor Value, 1% (kΩ)
51h	0.0
52h	12.1
53h	20.0
54h	28.0
55h	35.7
56h	44.2
57h	52.3
58h	open

### Restricted Address

The DCM also responds to address 0x50, but this address is for factory use only and cannot be used for any of the supported commands in the list below. This address is fixed and cannot be changed, so care must be taken that no other device on the bus uses address 0x50 in order to avoid address collisions.

## Supported Command List and Supported Commands Transaction Type

Command Name	Command Code	Function	Default Data Content	SMBus Write Transaction	SMBus Read Transaction	Number Data Bytes	Data Format
CLEAR_FAULTS	03h	Clear fault status register	n/a	Send Byte	n/a	0	bit
STORE_USER_CODE	17h	Can write VOUT_COMMAND to NV memory	n/a	Write Byte	n/a	1	bit
CAPABILITY	19h	DCM key capabilities set by factory	A0h	n/a	Read Byte	1	bit
VOUT_MODE	20h	Format for VOUT_COMMAND	17h	n/a	Read Byte	1	bit
VOUT_COMMAND	21h	Set DCM output voltage	1866h	Write Word	Read Word	2	ULINEAR16
STATUS_BYTE	78h	Fault Readback	n/a	n/a	Read Byte	1	bit
STATUS_WORD	79h	Generic Fault Readback	n/a	n/a	Read Word	2	bit
READ_VIN	88h	DCM Input Voltage	n/a	n/a	Read Word	2	LINEAR11
READ_VOUT	8Bh	Regulator Output Voltage at +INV terminal	n/a	n/a	Read Word	2	ULINEAR16
READ_IOUT	8Ch	DCM output current	n/a	n/a	Read Word	2	LINEAR11
READ_TEMPERATURE_1	8Dh	DCM Temperature at Regulator Controller	n/a	n/a	Read Word	2	LINEAR11
MFR_ID	99h	Manufacturer ID	"VI"	n/a	Block Read	2	ASCII
IC_DEVICE_ID	ADh	Device identification	"5100014"	n/a	Block Read	7	ASCII
MFR_STATUS_FAULTS	F0h	DCM-Specific Faults	n/a	n/a	READ 32	4	bit

## PMBus Command Definitions

A summary of the PMBus commands supported by the DCM are described in the following sections.

### CLEAR\_FAULTS Command (03h)

This command clears all status bits that have been previously set. Persistent or active faults are re-asserted again once cleared, except the “FLT falling edge” bit, which is edge-triggered. All faults are latched once asserted in the DCM. Registered faults will not be cleared when DCM powertrain is disabled through the  $\overline{\text{FLT}}$  or EN terminal.

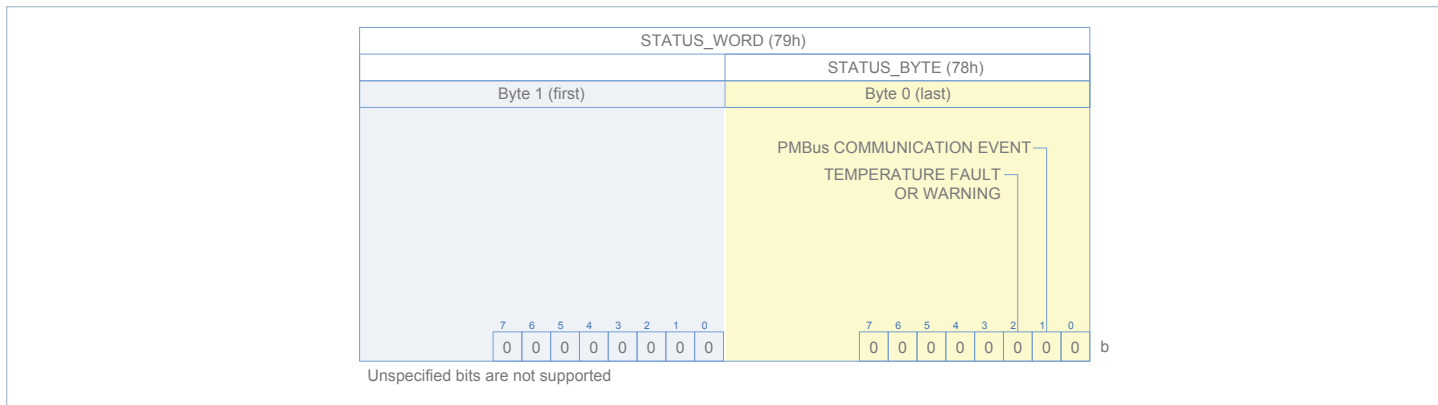
### STORE\_USER\_CODE Command (17h)

STORE\_USER\_CODE can save the VOUT\_COMMAND value to non-volatile memory. At subsequent power ups, this stored value is used for the DCM output voltage trim set point.

The data for STORE\_USER\_CODE is the command code to be stored; the DCM can only accept command code VOUT\_COMMAND (20h) to be stored.

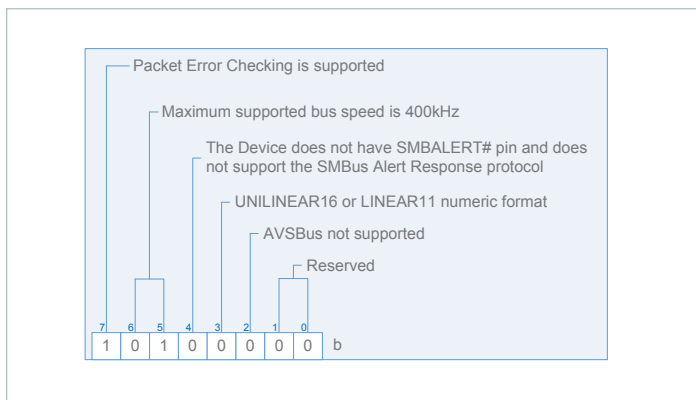
STORE\_USER\_CODE can only be used  $N_{\text{STORE\_USER\_CODE}}$  times before all non-volatile memory is consumed.





### CAPABILITY Command (19h)

The DCM returns a default value of A0h. This value indicates that the Packet Error Checking (PEC) is supported, PMBus® frequency is up to 400kHz, the SMBALERT# bit is not supported and that the numeric data can be LINEAR11 or ULINEAR16. See supported data command table indicating each command respective data reporting format.



### VOUT\_MODE Command (20h)

The DCM VOUT\_MODE command is read only; set to a default value of 17h.

### VOUT\_COMMAND Command (21h)

VOUT\_COMMAND causes the DCM to set the output voltage to the commanded value. When multiple DCMs are used in parallel to create a high-power array, the group command protocol should be used when using VOUT\_COMMAND to change the output voltage. The group command protocol allows for a PMBus command to be sent to multiple units in succession but halts execution by each module until the last command has been sent. This will cause all of the DCMs in the array to wait until the last VOUT\_COMMAND has been sent before collectively updating their output voltage setting. Not using the group command protocol can lead to nuisance detection of  $\%_{E_{AIN\_HI}}$  faults for units which are programmed lower than the others in the array.

### READ\_IOUT Command (8Ch)

READ\_IOUT returns the output current telemetry in LINEAR11 format.

### STATUS\_BYTE (78h) and STATUS\_WORD (79h)

Although the DCM powertrain will self-restart once fault conditions are cleared, all fault or warning flags, if set, will remain asserted until cleared by the host or once DCM input power is removed. This includes overtemperature warning and communication faults.

STATUS\_WORD and STATUS\_BYTE can be cleared by sending CLEAR\_FAULTS (03h) command.

The TEMPERATURE FAULT bit reflects that an overtemperature shut down of the Stage 1 ZVS buck-boost occurred.

The PMBus COMMUNICATION EVENT bit (CML) is set when a communication fault occurs. See the PMBus Communication Fault section for details.

### READ\_VIN Command (88h)

READ\_VIN returns the input voltage telemetry in LINEAR11 format.

### READ\_VOUT Command (8Bh)

READ\_VOUT returns the output voltage telemetry in ULINEAR16 format. Refer to the PMBus Power System Management Protocol Specification – Part II – Revision 1.3 for details on reported LINEAR11 and ULINEAR16 numeric format. READ\_VOUT telemetry is taken from the +INV node, so it will nominally read 4x the actual  $V_{OUT}$  during operation. Also note that there is a diode-clamp path from +OUT back to +INV, so when the module is disabled or the stage 2 current multiplier is stopped, READ\_VOUT will report a value equal to +OUT minus approximately 0.6V.

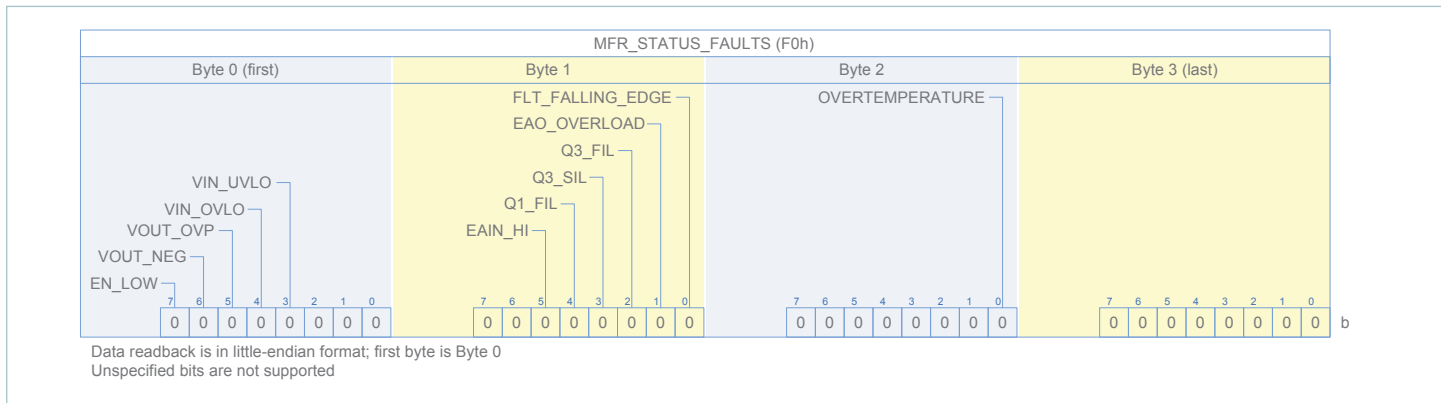
### READ\_TEMPERATURE\_1 (8Dh)

READ\_TEMPERATURE\_1 returns the measured temperature at the stage 1 ZVS buck-boost controller. This temperature can be used as a relative gauge to the operating temperature of one internal area of the module.

READ\_TEMPERATURE\_1 is not sufficient to design or validate any module-level thermal solution. Thermal design must use the module power dissipation and thermal resistance model to ensure that all areas of the module internal circuitry are kept below the maximum operating temperature.

### MFR\_ID (99h)

This read-only command will return "VI" as two ASCII bytes, indicating the manufacturer Vicor Corporation.



**MFR\_STATUS\_FAULTS (F0h)**

This command returns four bytes; the first three are used and are defined in the table above.

All fault or warning flags, if set, will remain asserted until cleared by the host using a CLEAR\_FAULTS (03h) command. CLEAR\_FAULTS should be issued after power is initially applied to clear any fault flags which are set during module initialization.

**PMBus Communication Fault**

**Module Behavior**

Corrupted data, unrecognized commands or other PMBus® protocol violations have no impact on powertrain functionality.

**PMBus Reporting Characteristics**

The below tables summarize data transmission and data content faults as implemented in the DCM.

Section	Description	STATUS_BYTE	Notes
		CML	
10.8.1	Corrupted data	X	PEC failure
10.8.2	Sending too few bits		Device will ignore transmission
10.8.3	Reading too few bits		No response
10.8.4	Host sends or reads too few bytes	X	CML set on writes only
10.8.5	Host sends too many bytes	X	
10.8.6	Reading too many bytes		Read will report old data
10.8.7	Device busy		Clock stretch prior to ACK

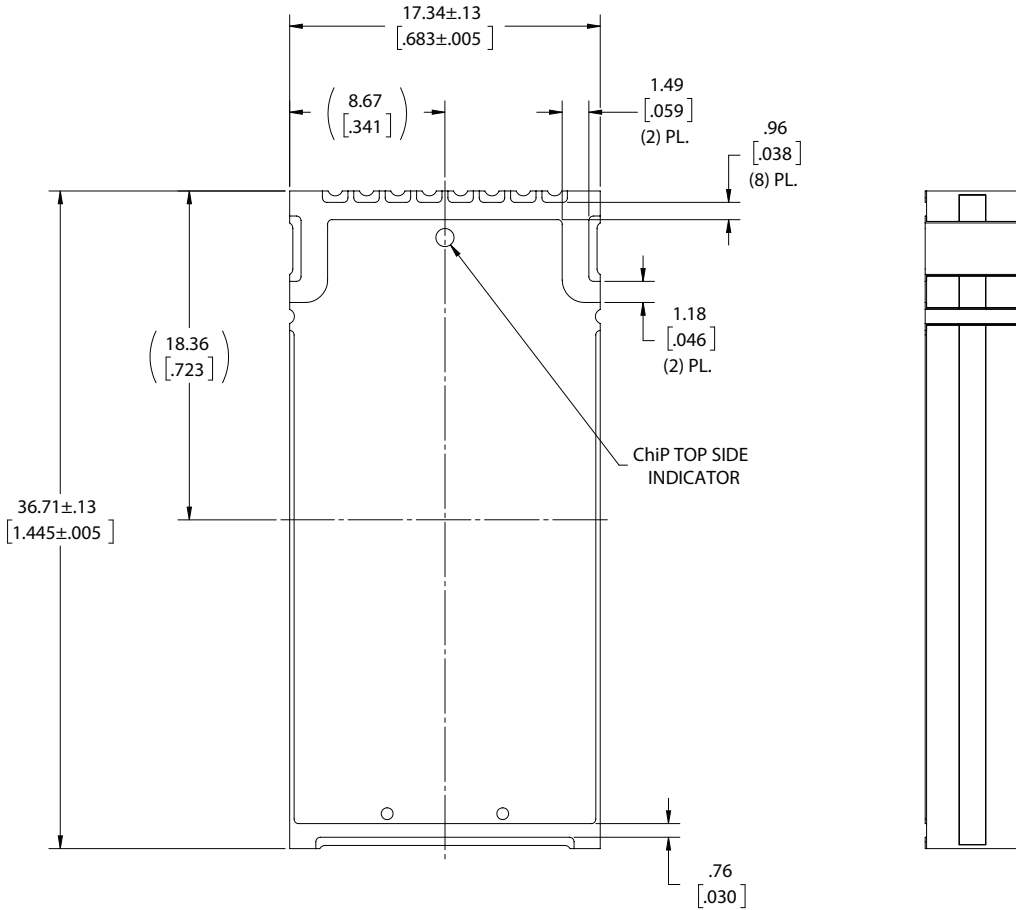
**Table 2** — Data transmission faults

Section	Description	STATUS_BYTE	Notes
		CML	
10.9.1	Improperly set read bit in the address byte		Not interpreted as a fault; Device will respond normally
10.9.2	Unsupported command code	X	
10.9.3	Invalid or unsupported data	X	
10.9.4	Data out of range		No response
10.9.5	Reserved bits		No response Not a fault

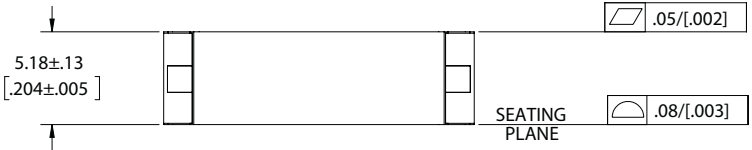
**Table 3** — Data content faults

Product Outline Drawing – Top View

DCM3717 TC3  
(Reference DWG # 53472 Rev 2)



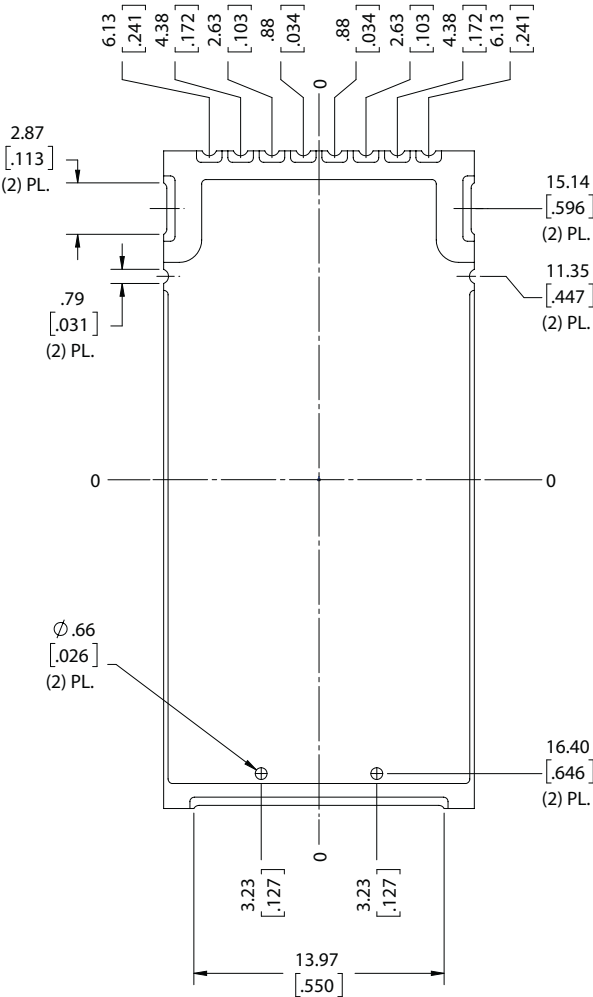
**TOP VIEW  
(COMPONENT SIDE)**



- NOTES:  
 1- UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE MM [INCH]  
 2- TOLERANCES ARE:  
 DECIMALS  
 X.XX [X.XX] = ±0.25 [0.01]  
 X.XXX [X.XXX] = ±0.127 [0.005]  
 ANGLES = ±1°

Product Outline Drawing – Bottom View

DCM3717 TC3  
(Reference DWG # 53472 Rev 2)

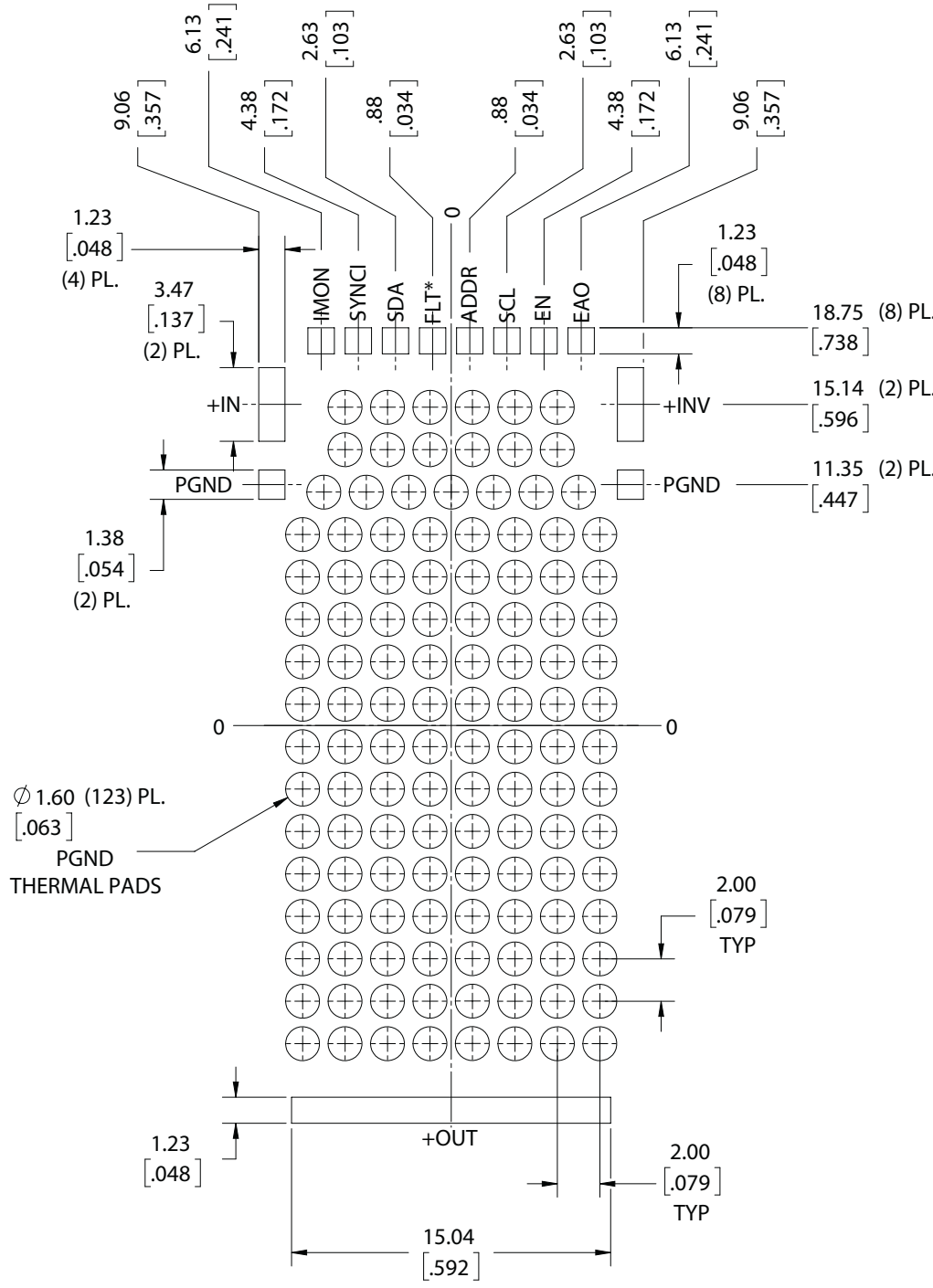


**BOTTOM VIEW**

Notes:  
1. Dimensional origin defined by package center. See package drawing top view.

Recommended Land Pattern

DCM3717 TC3  
(Reference DWG # 53472 Rev 2)



RECOMMENDED LAND PATTERN  
(COMPONENT SIDE)

- Notes:
1. Dimensional origin defined by package center. See package drawing top view.

Revision History

Revision	Date	Description	Page Number(s)
1.0	10/27/23	Initial release	n/a
1.1	11/30/23	Data sheet corrections	4, 24

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