PRM™ Regulator
PRM3735S58G54L5AB3

ZVS High-Efficiency Regulator

Features & Benefits

- Wide input range 31 – 58V_{DC}
- Wide output range 36 – 54V_{DC}
- 99.2% peak efficiency (48V input, 48V output)
- Up to 2.5kW continuous operation
- 262.4kW/L power density
- Thermally-adept SM-ChiP package
- PMBus®-compatible telemetry
- Internal voltage, current and temperature shut down
- Constant-current operation for battery charging
- Automotive APQP process + product development integration
- Integrated AECQ-100 qualified Vicor controller

Typical Applications

- Electric and Mild-Hybrid Vehicles
- Decentralized Architecture

Product Ratings	
V_{IN} = 31.0 – 58.0V	P_{OUT} = 2500W
V_{OUT} = 48V (36.0 – 54.0V Trim)	I_{OUT} = 52.1A

Product Description

The PRM3735 is a high-efficiency regulator converting a wide-range 31 – 58V_{DC} input into a regulated 48V_{DC} output with output power capability up to 2.5kW. The ZVS buck-boost topology enables high switching frequency operations with high conversion efficiency. High switching frequency allows for reduced-size reactive components, enabling high power density.

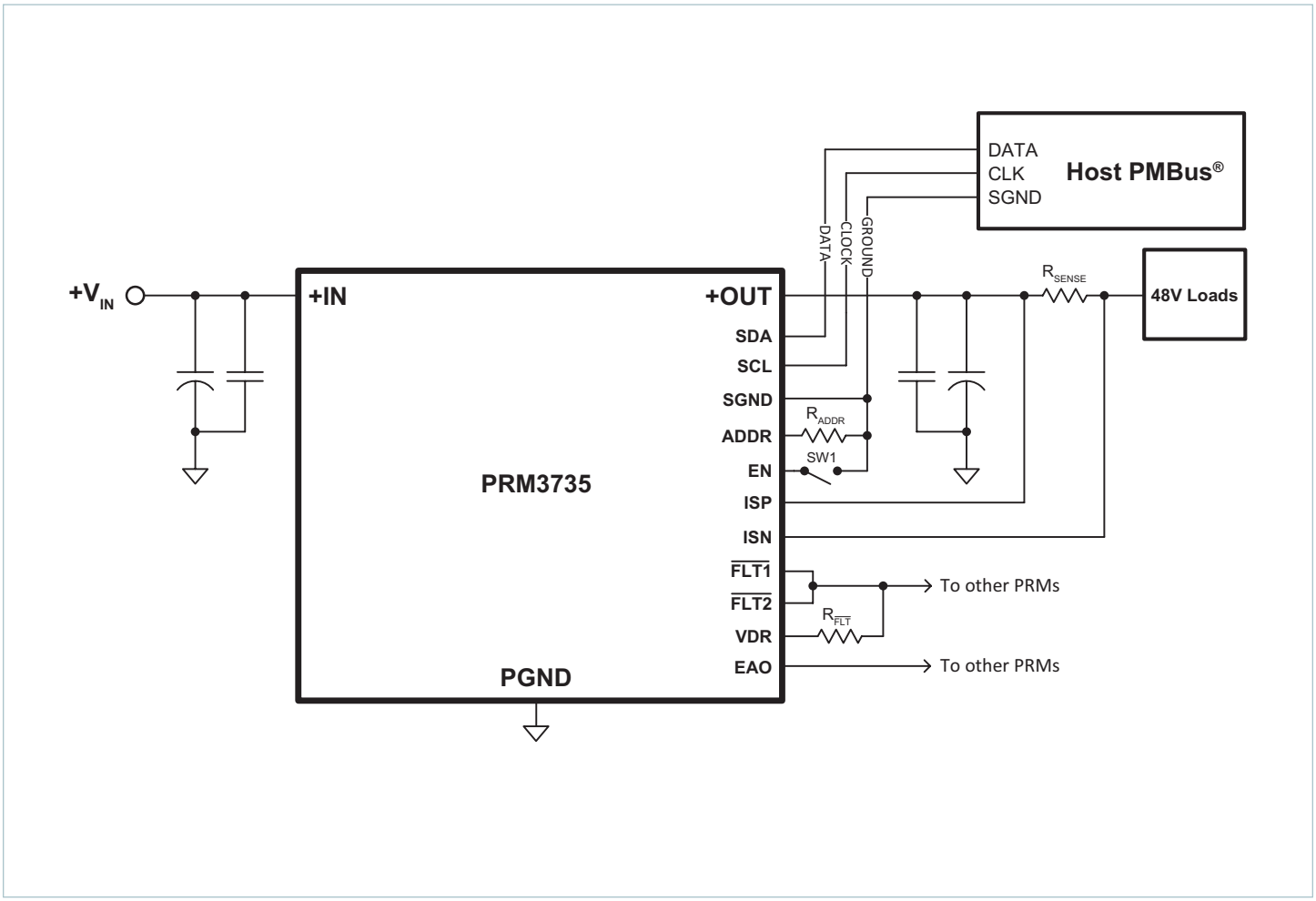
The SM-ChiP package is compatible with standard pick-and-place and surface-mount assembly processes with planar thermal-interface area and superior thermal conductivity.

Package Information

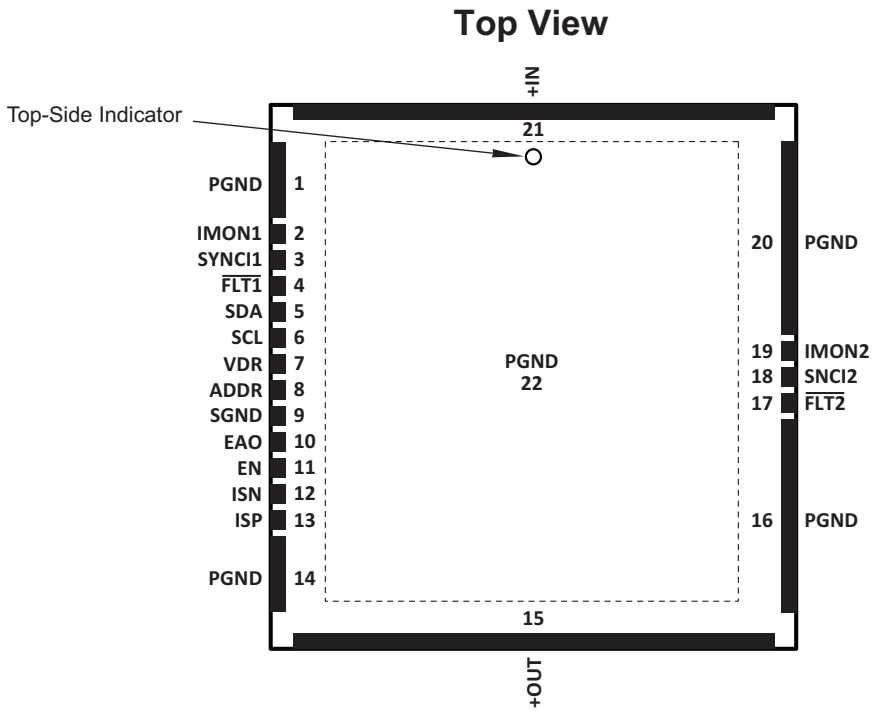
- 36.6 x 35.4 x 7.4mm SM-ChiP™
- Weight: 40g

Note: Product images may not highlight current product markings and cosmetic features.

Typical Application



Terminal Configuration



Terminal Descriptions

Signal Name	Terminal Number	Function
PGND	1, 14, 16, 20, 22 [a]	Power Ground: power return for +IN and +OUT current
IMON1	2	Factory use only; leave floating
SYNCI1	3	Factory use only; leave floating
$\overline{\text{FLT1}}$ [b]	4	Open-Drain Fault Flag: high impedance when regulator is operating normally; must be connected to $\overline{\text{FLT2}}$ on PCB
SDA	5	Digital serial communication data
SCL	6	Digital serial communication clock
VDR	7	Bias Supply Output: see Application Description for important considerations
ADDR	8	Digital serial communication address assignment
SGND	9	Signal Ground: reference for control signals; internally connected to PGND
EAO	10	Input to Powertrain Control Node
EN	11	Enable: when input asserted active or left floating, regulator is enabled
ISN	12	High-Side Current Sense Negative Input
ISP	13	High-Side Current Sense Positive Input
+OUT	15	Positive Output: power terminal
$\overline{\text{FLT2}}$ [b]	17	Open-Drain Fault Flag: high impedance when regulator is operating normally; must be connected to $\overline{\text{FLT1}}$ on PCB
SYNCI2	18	Factory use only; leave floating
IMON2	19	Factory use only; leave floating
+IN	21	Positive Input: power terminal

[a] Terminal 22 represents the package top and bottom conductive plating. Refer to product outline for additional details.
[b] Overbar ($\overline{\text{FLT}}$) or star (FLT*) marking signify an active low designation.

Part Ordering Information

Part Number	Temperature Grade	Tray Size
PRM3735S58G54L5**AB3**	**A** = –40 to 125°C	323 x 136 x 12mm 12 parts per tray Vicor PN 49556

Storage and Handling Information

Note: For compressive loading refer to Application Note AN:036, "Recommendations for Maximum Compressive Force of Heat Sinks."
For handling and assembly processing, and for rework considerations refer to Application Note AN:701, "SM-ChiP Reflow Soldering Recommendations."

Attribute	Comments	Specification
Storage Temperature Range		–40 to 125°C
Operating Internal Temperature Range (T_{INT})		–40 to 125°C
Weight		40g
MSL Rating		MSL 4, 245°C maximum reflow temperature
ESD Rating	Human Body Model JEDEC JS-001-2023	Class 2 ≥2kV
	Charged Device Model JEDEC JS-002-2022	Class 2a ≥500V

Reliability and Agency Approvals

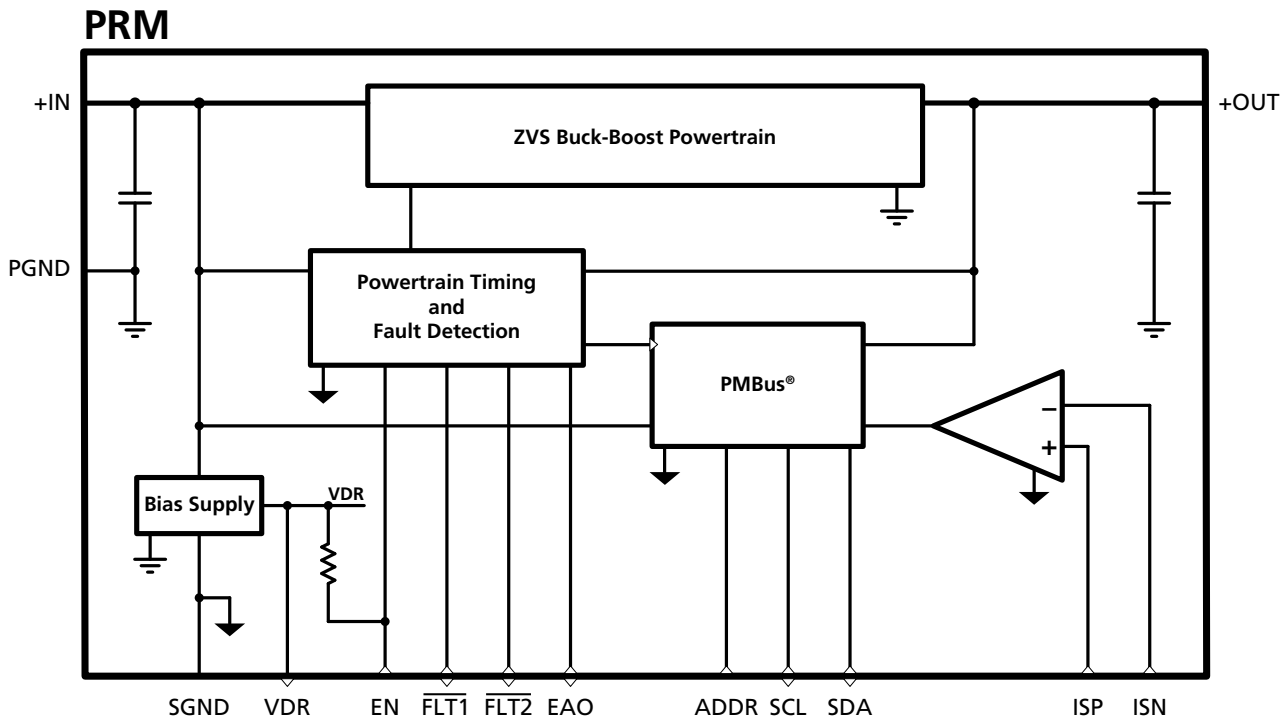
Attribute	Comments	Value	Unit
MTTF	MIL-HDBK-217F Parts Count, Ground Benign	4	MHrs
	MIL-HDBK-217F Parts Count, Ground Mobile	0.9	
FIT	MIL-HDBK-217F Parts Count, Ground Benign	232	FIT
	MIL-HDBK-217F Parts Count, Ground Mobile	1160	
Agency Approvals/Standards			

Absolute Maximum Ratings

The ABSOLUTE MAXIMUM ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to device. Electrical specifications do not apply when operating beyond rated operating conditions. Operating beyond rated operating conditions for an extended period of time may affect device reliability. Positive terminal currents represent current flowing out of the terminal.

Parameter	Comments	Min	Max	Unit
+IN to PGND	Continuous, non-operating	–0.5	70	V
+OUT to PGND	Continuous, non-operating	–0.5	70	V
VDR to SGND		–0.5	5.5	V
			100	mA
$\overline{FLT}$ to SGND		–0.5	5.5	V
		–20	20	mA
EN to SGND		–0.5	5.5	V
SCL to SGND		–0.5	5.5	V
SDA to SGND		–0.5	5.5	V
ISP to ISN		–0.3	0.5	V
ISP to SGND		–0.5	70	V
ISN to SGND		–0.5	70	V
EAO to SGND		–0.5	5.5	V
SGND		–100	100	mA

Functional Block Diagram



Electrical Specifications

Specifications apply over all line, trim and load conditions unless otherwise noted. **Boldface** specifications apply over the temperature range of –40°C ≤ T_{INT} ≤ 125°C and are assured to meet performance specification by design, test correlation, characterization and/or statistical process control. All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Input Specifications						
Input Voltage Range	V_{IN}	Typical value defines product V_{IN-NOM}	**31**	48	**58**	V
Input Voltage Slew Rate	dV_{IN}/dt	0V ≤ V_{IN} ≤ 58.0V			**1**	V/µs
Input Voltage for ADDR Latch	V_{IN_ADDR}	Initial power up			**12**	V
Input Voltage for ADDR Latch	V_{IN_ADDR}	Initial power up			**12**	V
No-Load Power Dissipation	P_{NL}	EN high, V_{IN} = 48.0V		0.67	**1.5**	W
Input Quiescent Current	I_{QC}	EN low, V_{IN} = 31.0V		10.0	**14.0**	mA
		EN low, V_{IN} = 48.0V		12.3	**17.2**	
		EN low, V_{IN} = 58.0V		13.9	**19.5**	
Input Current	I_{IN_DC}	I_{OUT} = 52.1A, V_{IN} = 48.0V, V_{OUT} = 48.0V		52.5	**53.2**	A
Input Capacitance (Internal)	C_{IN_INT}	Effective value, V_{IN} = 48.0V		20.8		µF
Input Capacitance (Internal) ESR	R_{C-IN}	Effective value, V_{IN} = 48.0V		0.29		mΩ
Power Output Specifications						
Output Voltage Trim Range	V_{OUT}	No load; typical value defines product $V_{OUT-NOM}$	**36**	48.0	**54**	V
Output Voltage Load Regulation	$V_{OUT\_REG\_LOAD}$			0.1	0.5	%
Output Voltage Line Regulation	$V_{OUT\_REG\_LINE}$			0.05	0.5	%
Rated Output Power, Continuous	P_{OUT}				**2500**	W
Rated Output Current, Continuous	I_{OUT}				**52.1**	A
Array Size	n_{ARRAY}	Guaranteed by design; array of two tested			**3**	PRMs
Switching Frequency	F_{SW}	V_{IN} = 54.0V, V_{OUT} = 48.0V, I_{OUT} = 26.1A, T_{INT} = 25°C	1.15	1.25	1.35	MHz
		Over rated line, rated load, trim and temperature, exclusive of burst mode	**0.4**		**1.35**	MHz
Output Turn-On Delay	t_{ON}	From V_{IN} first crossing $V_{IN-UVLO+}$ to soft-start ramp		23		ms
		From EN release to soft start ramp, V_{IN} pre-applied		4.4		
Output Voltage Rise Time	$t_{RISE-VOUT}$	From soft start begin to V_{OUT} settled to within 5%	**70**	90	**110**	ms
Efficiency, Ambient	η_{AMB}	V_{IN} = 48.0V, V_{OUT} = 48.0V, I_{OUT} = 52.1A, T_{CASE} = 25°C	98.2	99.2		%
		V_{IN} = 31.0 – 58.0V, V_{OUT} = 48.0V, I_{OUT} = 52.1A, T_{CASE} = 25°C	94.6			
		V_{IN} = 31.0 – 58.0V, I_{OUT} = min (smaller of 52.1A or 2500W/V_{OUT}), T_{CASE} = 25°C, over trim	94.2			
Efficiency, Hot	η_{HOT}	V_{IN} = 48.0V, V_{OUT} = 48.0V, I_{OUT} = 52.1A, T_{CASE} = 80°C	97.9	99.1		%
		V_{IN} = 31.0 – 58.0V, V_{OUT} = 48.0V, I_{OUT} = 52.1A, T_{CASE} = 80°C	94.2			
		V_{IN} = 31.0 – 58.0V, I_{OUT} = min (smaller of 52.1A or 2500W/V_{OUT}), T_{CASE} = 80°C, over trim	93.5			
Efficiency Over Temperature	η	V_{IN} = 31.0 – 58.0V, V_{OUT} = 48.0V, >50% rated load current	**94.0**			%
		V_{IN} = 31.0 – 58.0V, >50% rated load current, over trim	**93.5**			

Electrical Specifications (Cont.)

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Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Output Specifications (Cont.)						
Output Discharge Current	I_{OD}	Average value, V_{OUT} = 0.5V		10		mA
Output Voltage Ripple	V_{OUT_PP}	V_{IN} = 54.0V, V_{OUT} = 48.0V, I_{OUT} = 26.1A, C_{OUT_EXT} = 18.8µF, 20MHz BW		0.42	**0.75**	V_{P-P}
Output Inductance (Parasitic)	L_{OUT}	F_{SW} = 1.25MHz, Simulated terminal model		3.4		nH
Output Capacitance (Internal)	C_{OUT_INT}	Effective value, V_{OUT} = 48.0V		20.8		µF
Output Capacitance (Internal) ESR	R_{COUT_INT}	Effective value, V_{OUT} = 48.0V		0.29		mΩ
Load Capacitance (External)	C_{LOAD}	At PRM output, V_{OUT} = 0V, ceramic only	**3.3**		**33**	µF
		At PRM output, V_{OUT} = 48.0V, electrolytic only	**0**		**1000**	
		At PRM output, V_{OUT} = 0V, ceramic with electrolytic ≥ 330µF	**0**		**330**	
Fault Detection and Response						
V_{IN} UVLO Threshold Rising	V_{IN_UVLO+}	Powertrain recovery	**24.4**	28.4	**30.5**	V
V_{IN} UVLO Hysteresis	$V_{IN\_UVLO\_HYS}$		**2.1**	2.6	**3.1**	V
V_{IN} OVLO Threshold Rising	V_{IN_OVLO+}	Powertrain recovery	**58.7**	61.7	**67**	V
V_{IN} OVLO Hysteresis	$V_{IN\_OVLO\_HYS}$		**1.0**	1.2	**1.4**	V
Output Overvoltage Shut Down	V_{OUT_OVP}		**56.1**	57.9	**62.10**	V
Minimum Current-Limited V_{OUT}	V_{OUT_UVP}				**31**	V
Overtemperature Shut Down	T_{OT}	Detected at control IC	125			°C
Overtemperature Restart Hysteresis	T_{OT_HYS}	Measured at control IC		30		°C
EAO Overload Limit	V_{EAO_LIMIT}		**3.2**	3.3	**3.4**	V
Output Overload Timeout	t_{EAO_OL}	EAO continuously above EAO_LIMIT		1		ms
Output Overvoltage Relative	$\%_{EAIN\_HI}$	Relative to the VOUT_COMMAND; inactive during start up and for t_{EAIN_HI} after a VOUT_COMMAND write	**4**	15		%
Output Overvoltage Relative Timout	t_{EAIN_HI}	Blanking time for Output Overvoltage Relative following VOUT_COMMAND write		2.1		s
Output Voltage Negative Fault Threshold	V_{OUT_NEG}	Level threshold to trigger fault	**–0.45**	–0.25	**–0.15**	V
Output Voltage Threshold to Re-Enable V_{OUT_NEG} Fault	$V_{OUT\_NEG\_RE-ARM}$	Positive-going V_{OUT} which re-arms the V_{OUT_NEG} fault	**1**	2.25	**3**	V
Fault Response Time	t_{FAULT}	OVLO, UVLO, ENABLE, OTP		2		µs
Fault Recovery Time	$t_{FAULT\_RECOVERY}$	OVLO, UVLO, OTP, VOUT_UV		40		ms

Electrical Specifications (Cont.)

Specifications apply over all line, trim and load conditions unless otherwise noted. **Boldface** specifications apply over the temperature range of –40°C ≤ T_{INT} ≤ 125°C and are assured to meet performance specification by design, test correlation, characterization and/or statistical process control. All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
PMBus® Telemetry Characteristics						
READ_VIN Accuracy	READ_VIN_ACC	Across all line, trim and load	**–5**		**5**	%
READ_VIN Resolution	READ_VIN_RES			125		mV
READ_VIN Functional Range	READ_VIN_RNG		**0**		**88**	V
READ_VOUT Accuracy	READ_VOUT_ACC	Across all line, trim and load	**–5**		**5**	%
READ_VOUT Resolution	READ_VOUT_RES			35.2		mV
READ_VOUT Functional Range	READ_VOUT_RNG		**0**		**88**	V
READ_IOUT Accuracy	READ_IOUT_ACC	Across all line, trim and load	**–10**		**10**	%
READ_IOUT Resolution	READ_IOUT_RES			62.5		mA
READ_IOUT Functional Range	READ_IOUT_RNG		**0.5**		**63.9**	A
READ_TEMPERATURE Accuracy	READ_TEMP_ACC	Disabled, with T_{CASE} = 25°C	**–6**		**6**	°C
READ_TEMPERATURE Functional Range	READ_TEMP_RNG		**–273**		**184**	°C
VOUT_COMMAND Accuracy	VOUT_COMMAND_ACC	Across all line and trim at no load	**–5**		**5**	%
VOUT_COMMAND Resolution	VOUT_COMMAND_RES			2		mV
VOUT_COMMAND Functional Range	VOUT_COMMAND_RNG		**36**		**54**	V
IOUT_OC_FAULT_LIMIT Accuracy	IOUT_OC_FAULT_LIMIT_ACC	Across all line and trim, >50% load	**–10**		**10**	%
IOUT_OC_FAULT_LIMIT Resolution	IOUT_OC_FAULT_LIMIT_RES	With 0.5mΩ shunt		0.5		A
		With 2mΩ shunt		0.25		
IOUT_OC_FAULT_LIMIT Functional Range	IOUT_OC_FAULT_LIMIT_RNG		**0.5**		**63.9**	A
VOUT_TRANSITION_RATE Accuracy	VOUT_TRANSITION_RATE_ACC	Across all line, trim, at no load	**–5**		**5**	%
VOUT_TRANSITION_RATE Resolution	VOUT_TRANSITION_RATE_RES			1		mV/µs
VOUT_TRANSITION_RATE Functional Range	VOUT_TRANSITION_RATE_RNG		**1**		**50**	mV/µs
STORE_USER_CODE Capacity	STORE_USER_CODE_CAP	Storage of user defined commands			**8**	Writes

Electrical Specifications (Cont.)

Specifications apply over all line, trim and load conditions unless otherwise noted. **Boldface** specifications apply over the temperature range of –40°C ≤ T_{INT} ≤ 125°C and are assured to meet performance specification by design, test correlation, characterization and/or statistical process control. All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Fault: $\overline{FLT}$						
Pull-up Voltage	$V_{\overline{FLT}\_INACTIVE}$	Minimum $R_{PULL-UP}$ to VDR = 10kΩ			**5.3**	V
Sink Current	$I_{\overline{FLT}\_ACTIVE}$	Fault active, $V_{\overline{FLT}}$ = 400mV	**4**			mA
Input Voltage Threshold	$V_{\overline{FLT}\_ACTIVE}$	To externally induce shut down	**0.85**		**1.1**	V
Serial Clock: SCL Serial Data: SDA						
Serial Voltage Range	V_{SERIAL}		3.3		5	V
Operating Frequency	F_{SMB}		**10**		**400**	kHz
Input High Threshold	V_{IH}		1.35			V
Input Low Threshold	V_{IL}				0.8	V
Output Low Threshold	V_{OL}				0.4	V
Clock Low Timeout	$t_{TIMEOUT}$	35ms clock stretching period supported	25		35	ms
Bias Supply: VDR						
VDR Start-Up Current	I_{VDR_STDBY}	Available source current during start up, VDR low			**1**	mA
VDR Input Undervoltage Turn-On	$V_{IN\_VDR\_UVLO+}$			4.7	**4.9**	V
VDR Turn-On Hysteresis	$V_{IN\_VDR\_UVLO\_HYST}$			0.2		V
VDR Turn-On Delay	t_{ON_VDR}	V_{IN} start from <1V, V_{IN} > $V_{IN\_VDR\_UVLO+}$ to VDR high		10.5	**30**	ms
VDR Voltage	V_{VDR}		**5**	5.3	**5.4**	V
VDR Source Current	I_{VDR_ON}	Available source current, VDR high, after t_{ON_VDR}			**100**	mA
Address: ADDR						
ADDR Registration Time	t_{SADDR}	From V_{IN} crossing V_{IN_ADDR}		10.5	**30**	ms
ADDR Pull-Up Current	I_{PULLUP_INIT}	During controller initialization		50		µA
ADDR Pull-Up Voltage	V_{PULLUP_OP}	Following t_{SADDR}		4.6		V
ADDR Source Current	I_{ADDR}	R_{ADDR} = 0Ω		50		µA
Control Node: EAO						
EAO Voltage Range	V_{EAO}	Across line, trim, load	**0**		**3.24**	V
EAO Current Drive	I_{EAO}		**300**		**600**	µA
EAO Pulse Skip Threshold	V_{EAO_SKIP}	Lower side of hysteretic range		0.4		V
EAO Sink Current	I_{EAO_SKIP}	Pull down to 0V		450		µA
Enable: EN						
EN Enable Threshold	$V_{ENABLE-EN}$		**1.1**			V
EN Disable Threshold	$V_{ENABLE-DIS}$				**0.7**	V
EN Pull-Up Resistor	R_{PULLUP_EN}	Internal pull-up resistor to VDR		10		kΩ

Specified Operating Area

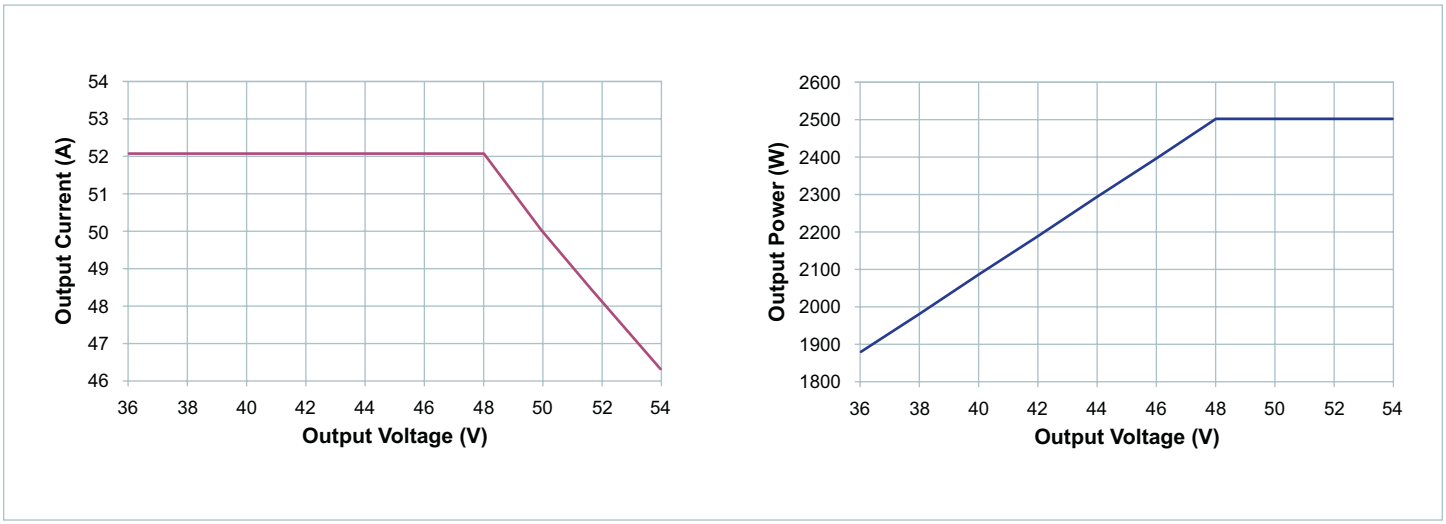


Figure 1 — *Specified electrical operating area using rated R_{LO}; T_{CASE} = 25°C*

Thermal Specified Operating Area

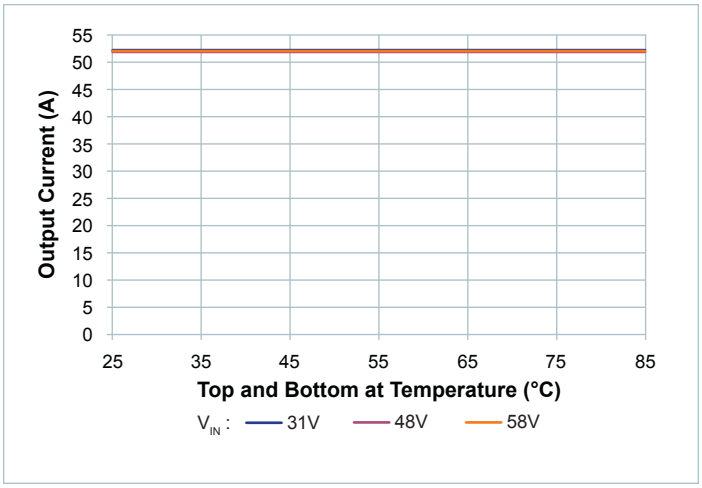


Figure 2 — *Thermal specified operating area at V_{OUT} = 36V: max system P_{OUT} vs. temperature at top bottom and leads*

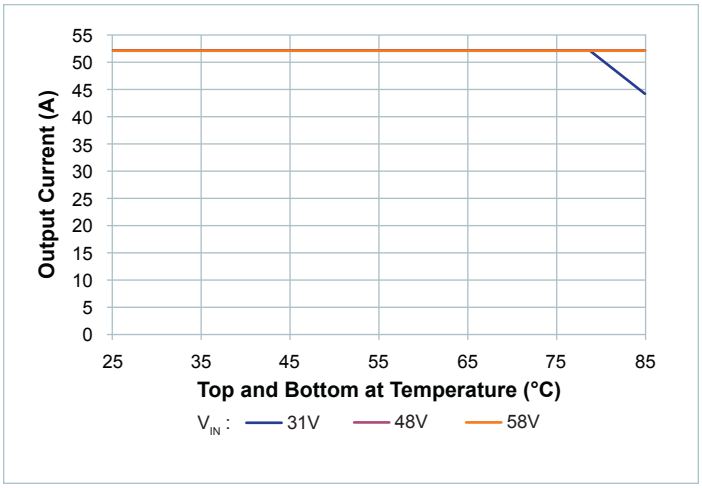


Figure 3 — *Thermal specified operating area at V_{OUT} = 48V: max system P_{OUT} vs. temperature at top bottom and leads*

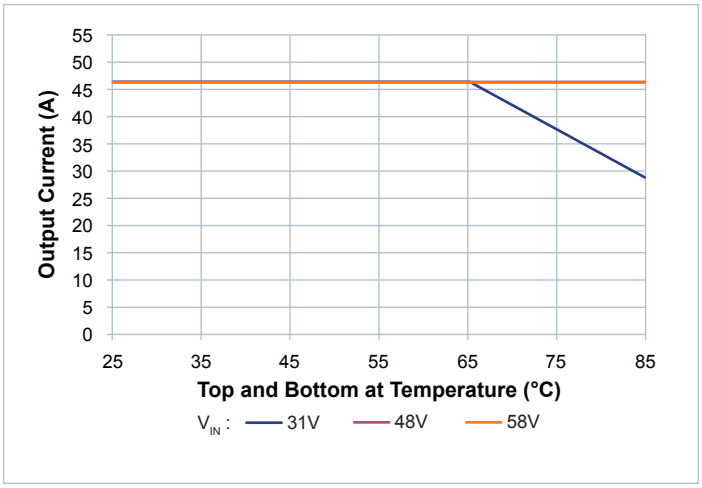


Figure 4 — *Thermal specified operating area at V_{OUT} = 54V: max system P_{OUT} vs. temperature at top bottom and leads*

Typical Performance Characteristics

The following figures present performance data in a typical application environment.

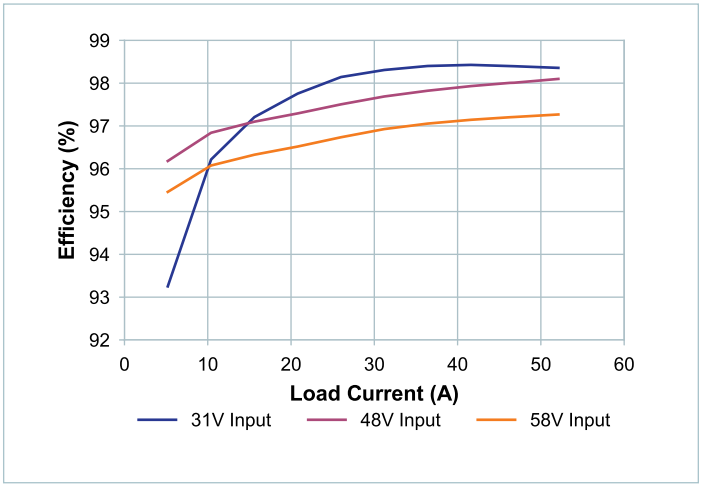


Figure 5 — *Efficiency at 25°C case temperature, V_{OUT} = 36V*

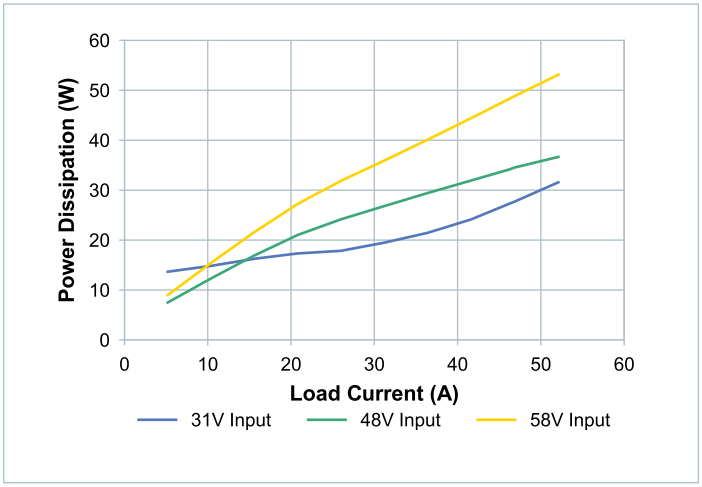


Figure 6 — *Power dissipation at 25°C case temperature, V_{OUT} = 36V*

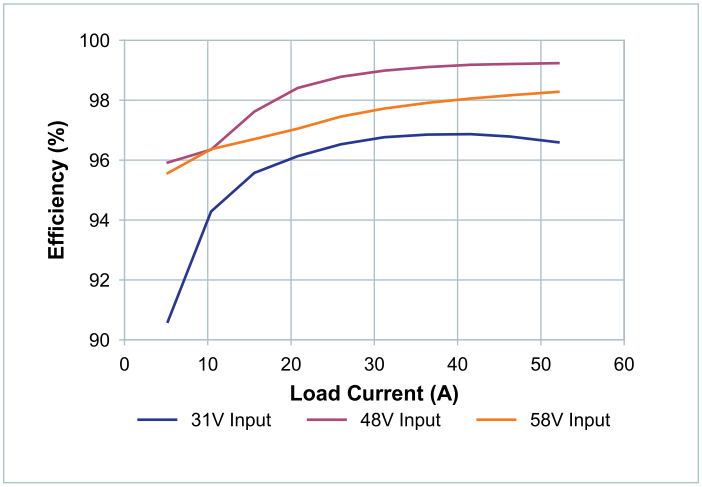


Figure 7 — *Efficiency at 25°C case temperature, V_{OUT} = 48V*

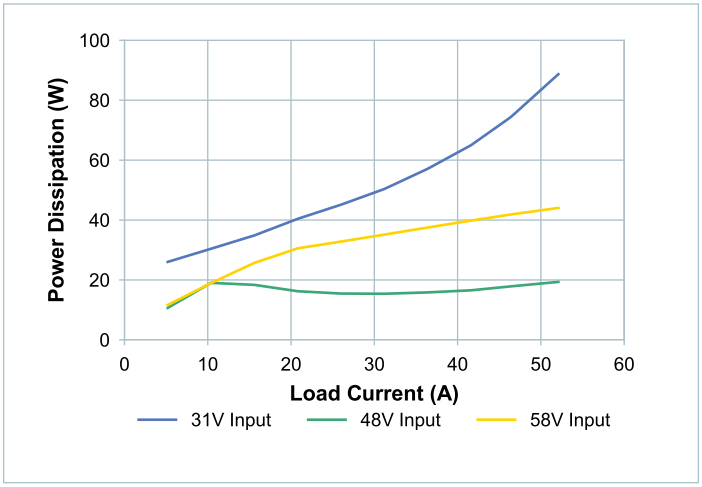


Figure 8 — *Power dissipation at 25°C case temperature, V_{OUT} = 48V*

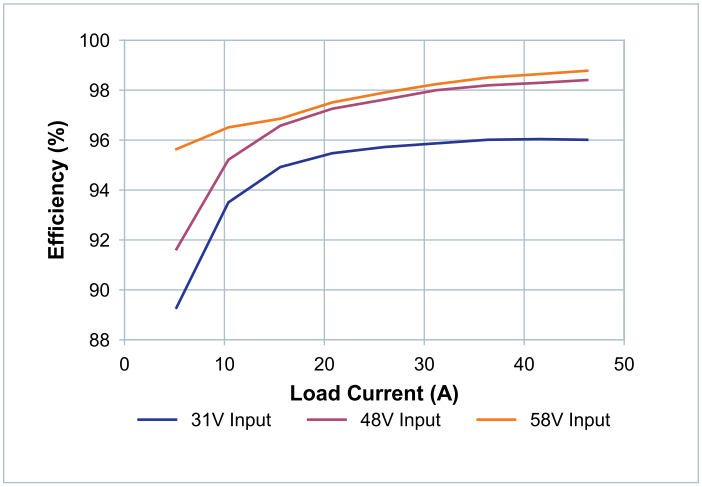


Figure 9 — *Efficiency at 25°C case temperature, V_{OUT} = 54V*

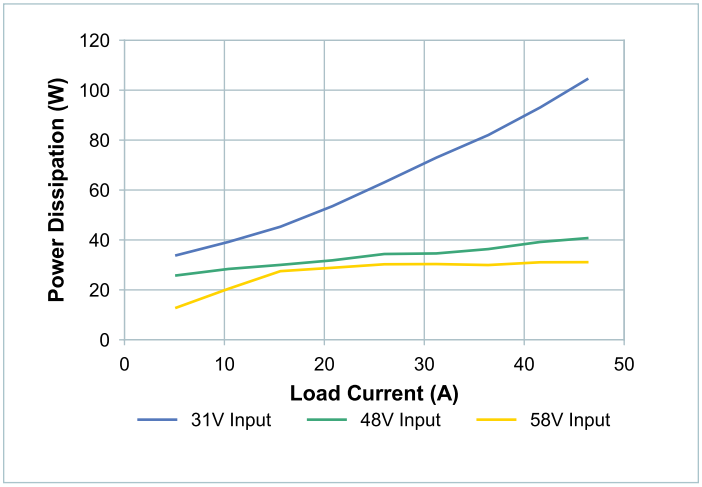


Figure 10 — *Power dissipation at 25°C case temperature, V_{OUT} = 54V*

Typical Performance Characteristics (Cont.)

The following figures present performance data in a typical application environment.

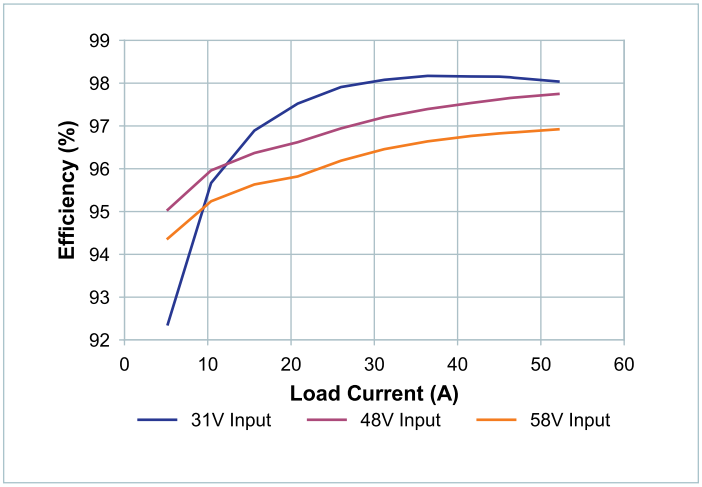


Figure 11 *— Efficiency at 85°C case temperature, V_{OUT} = 36V*

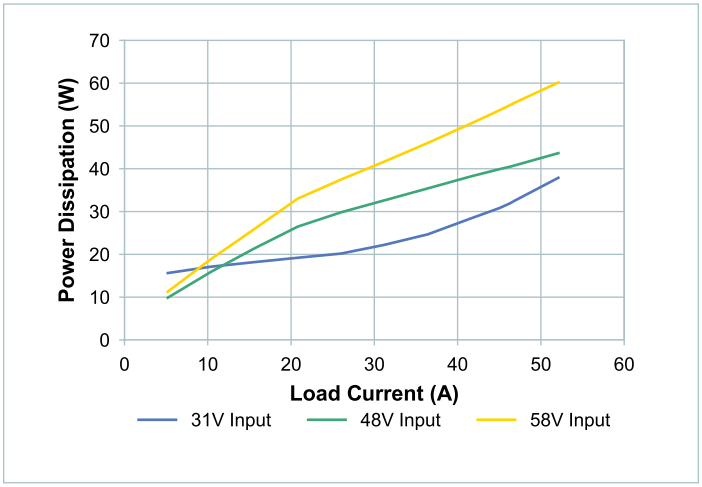


Figure 12 *— Power dissipation at 85°C case temperature, V_{OUT} = 36V*

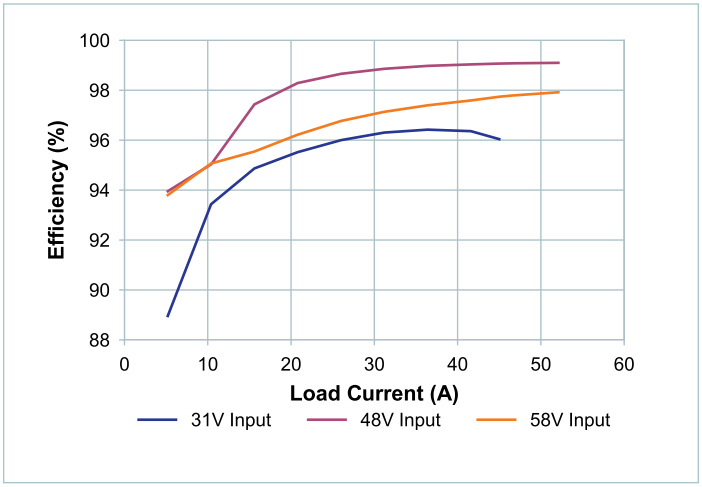


Figure 13 *— Efficiency at 85°C case temperature, V_{OUT} = 48V*

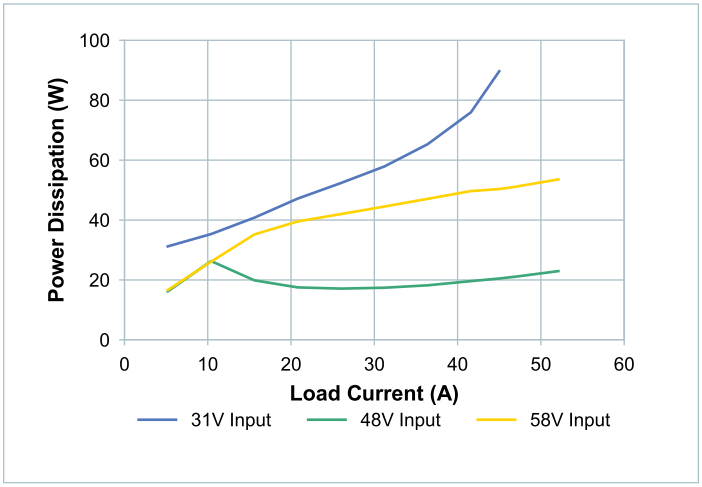


Figure 14 *— Power dissipation at 85°C case temperature, V_{OUT} = 48V*

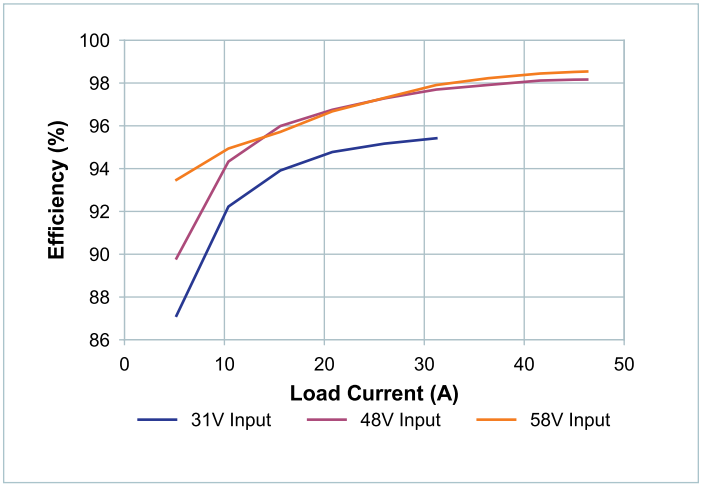


Figure 15 *— Efficiency at 85°C case temperature, V_{OUT} = 54V*

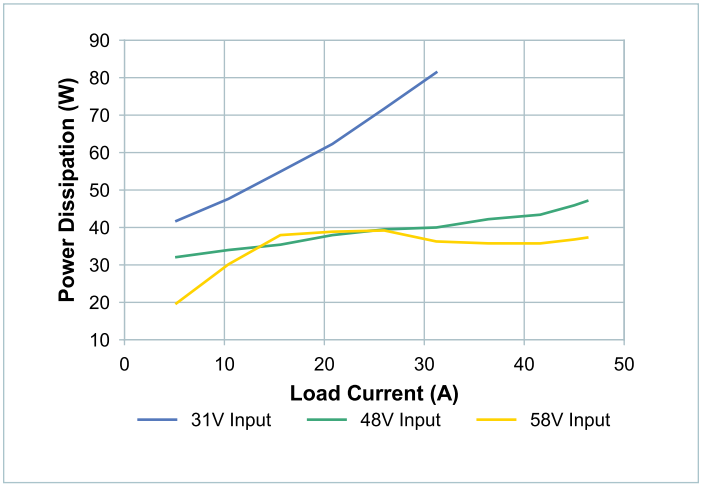


Figure 16 *— Power dissipation at 85°C case temperature, V_{OUT} = 54V*

Typical Performance Characteristics (Cont.)

The following figures present performance data in a typical application environment.

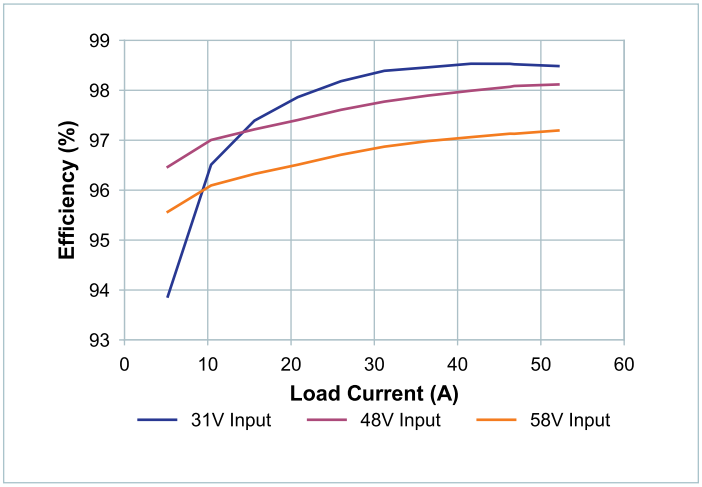


Figure 17 — *Efficiency at –40°C case temperature, V_{OUT} = 36V*

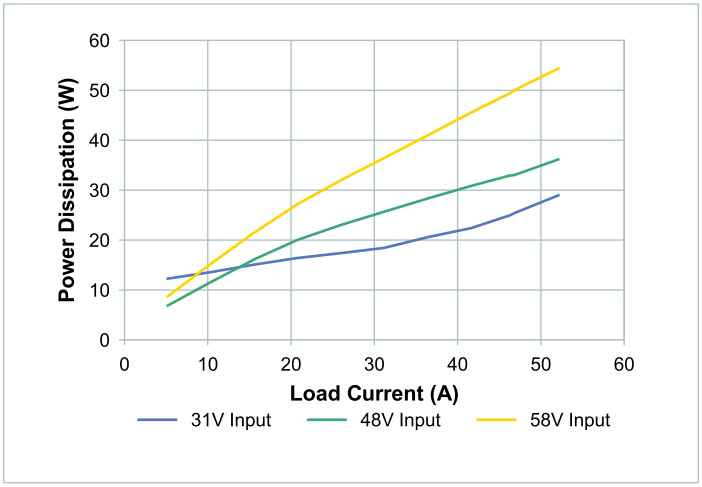


Figure 18 — *Power dissipation at –40°C case temperature, V_{OUT} = 36V*

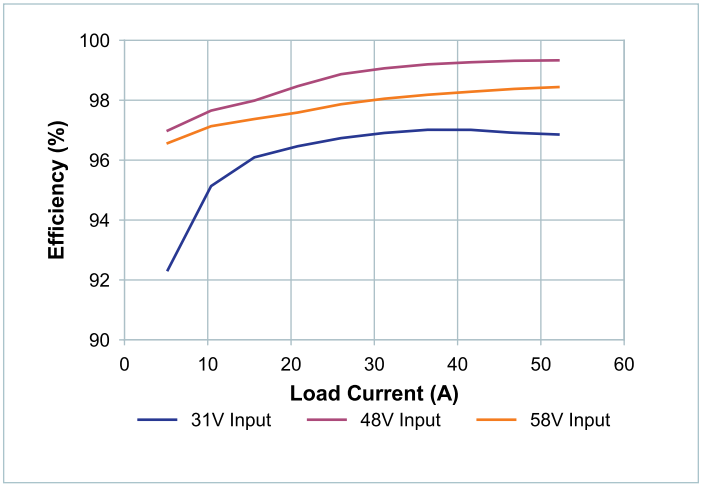


Figure 19 — *Efficiency at –40°C case temperature, V_{OUT} = 48V*

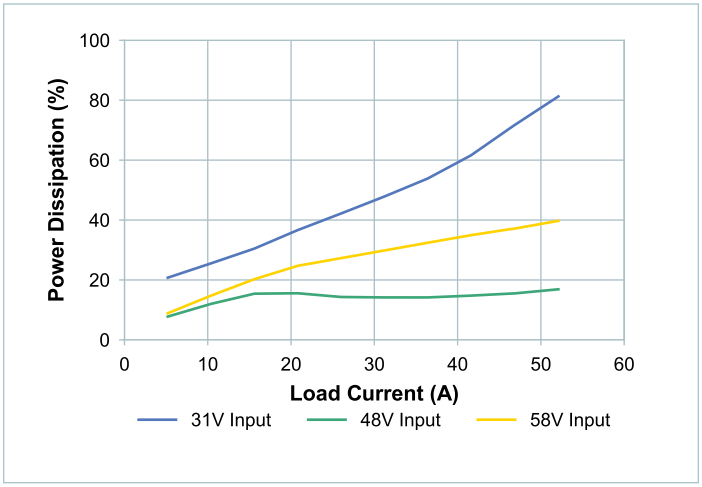


Figure 20 — *Power dissipation at –40°C case temperature, V_{OUT} = 48V*

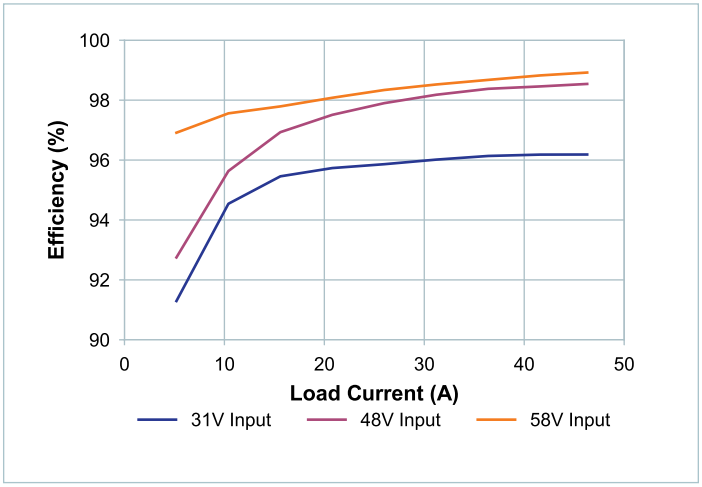


Figure 21 — *Efficiency at –40°C case temperature, V_{OUT} = 54V*

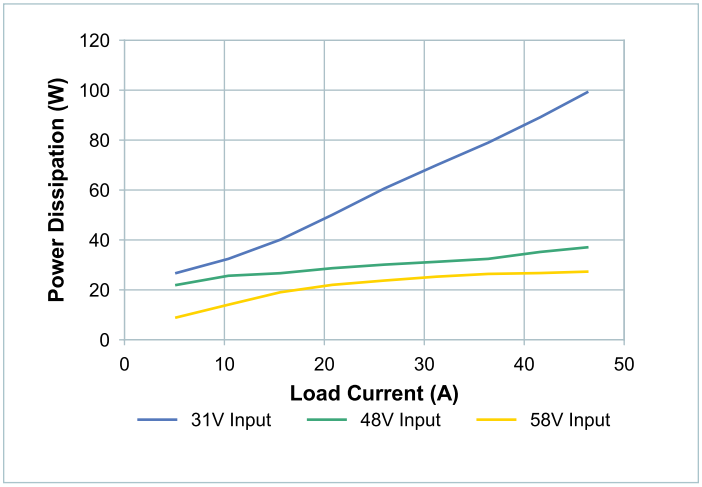


Figure 22 — *Power dissipation at –40°C case temperature, V_{OUT} = 54V*

Terminal Functions

VDR – Bias Regulator

The VDR internal bias regulator is an internally-generated 5V supply, which is intended primarily to power the internal controller and driver circuitry. VDR can be loaded up to I_{VDR_ON} once the device has completed start up. During start up the load on VDR must be limited to I_{VDR_STDBY}.

+IN – Input Power

The +IN terminal is the power rail input to the PRM. External filtering and decoupling techniques are application-specific. Low-ESR ceramic capacitors are recommended at the input terminal to power ground.

+OUT – Output Power

The +OUT terminal is the power rail output of the PRM. External filtering and decoupling techniques are application-specific. Low-ESR ceramic capacitors are recommended at the output terminal to power ground.

EAO – Modulator

EAO is the error amplifier output and is used for current sharing when parts are operated in an array. The module compensation is pre-programmed by the factory and is internal to the device.

EN – Enable

The EN terminal of the regulator is referenced to SGND and permits the user to turn the regulator on or off. The EN polarity is a positive logic assertion. If the EN terminal is left floating or asserted high, the regulator output is enabled. When EN is asserted low, the regulator will complete the current switching cycle and enter a low-power state until EN is released.

ADDR, SCL, SDA

Address (ADDR) is a multi-level analog input which sets the address at initial power-up.

Serial clock (SCL) and serial data (SDA) require external pull-up resistors for normal operation. Refer to System Management Bus (SMBus) Specification version 3.0 for details.

SGND – Signal Ground

SGND provides a Kelvin connection to PGND within the PRM for accurate control and monitoring of the package signal terminals. SGND must be used as the reference for all signal and control terminals. SGND must not be connected to PGND outside the PRM package or the benefits of the Kelvin connection will be lost.

PGND – Power Ground

PGND is the common power return.

IMON1, IMON2 – Factory Use Only

Do not connect to the SYNCI terminal.

$\overline{FLT1}$, $\overline{FLT2}$ – Fault Monitoring

$\overline{FLT1}$ and $\overline{FLT2}$ are open-drain terminals for indication of powertrain fault status. Interconnect $\overline{FLT1}$ and $\overline{FLT2}$ on the application PCB. The $\overline{FLT1}$ and $\overline{FLT2}$ terminals are not internally pulled up to bias voltage. An external pull-up resistor, $R_{\overline{FLT}}$, is required to VDR terminal when used as a standalone regulator (10kΩ recommended). In an array of PRMs, $\overline{FLT}$ terminals must be interconnected to synchronize start up and fault response.

$\overline{FLT1}$ and $\overline{FLT2}$ are active-low, so when any fault shut down is active the signals will drive low. When the module is enabled and not in a fault condition, the signals will be allowed to float high. The module monitors the status of this terminal, and so if an external sub-circuit pulls $\overline{FLT}$ low, the module will also be disabled.

Note: $\overline{FLT}$ displayed as FLT* on the package drawing.

ISP, ISN – Current-Sense Inputs

Differential current monitor input for high-side current sense amplifier. Connect across high-side current-sense resistor in +OUT path. For rated power application, use current-sense resistor R_{SENSE} = 500µΩ, 1% tolerance.

SYNCI1, SYNCI2 – Factory Use Only

Do not connect to the SYNCI terminal.

Functional Description

The PRM is a non-isolated, ZVS buck-boost DC-DC power converter with PMBus® telemetry in a thermally-adept package.

Analog EN Terminal Operation

The analog EN terminal enables and disables the PRM; when pulled low by an external supervisor circuit, the unit will be disabled. The EN terminal is internally pulled high; when left floating or driven high externally, the PRM is enabled.

The EN terminal is referred to the SGND terminal of the PRM signal terminal interface. Note that the SGND terminal and the PGND low-voltage-side power return terminals are common. To avoid noise interference, the SGND signal must be kept separate from the PGND in the electrical design and circuit layout.

The $\overline{FLT}$ terminal will be logic low during when the powertrain is disabled via the analog EN terminal. Upon enabling the module, the $\overline{FLT}$ terminal will be asserted high at the beginning of soft-start.

The analog EN terminal status is registered by the PMBus telemetry and reporting interface. In byte 3 of MFR_FAULT_STATUS (F0h), the EN_PIN_LOW bit is asserted when the EN terminal is pulled low.

All fault flags, if set, will remain asserted until cleared by the host or once the PRM input power is removed.

PRM powertrain operation status is indicated in the high byte of STATUS_WORD (79h). The POWER_GOOD# bit is set, anytime the PRM is not in the enabled state, to indicate that the powertrain is inactive and not switching. The POWER_GOOD# bit is cleared, when the PRM is in the active and enabled state, after the powertrain is active and soft-start has elapsed. The POWER_GOOD# bit cannot be cleared as it always reflects the current state of the module.

PRM Fault Response

If the PRM detects a fault, it pulls the $\overline{FLT}$ terminal low within t_{FAULT} and the powertrain stops at the end of the current switching cycle. Once the fault recovery time ($t_{FAULT\text{-}RECOVERY}$) elapses and the fault is no longer present, the PRM resumes operation according to EAO.

Input undervoltage, input overvoltage, overtemperature, EN or $\overline{FLT}$ terminals low and output overvoltage faults are all level-sensitive. The PRM will not attempt to start again after shut down as long as the fault is present, and will hold $\overline{FLT}$ low continuously. Note that $\overline{FLT}$ being held (externally) low will also inhibit restart of the PRM.

Other fault types like output voltage negative, output overcurrent or EAO_OL can normally only occur when the module is operating. After shut down due to one of these faults, the PRM will attempt a restart after the fault recovery time, but may shut down repeatedly for as long the load fault condition persists.

Input Undervoltage Recovery and Lockout Thresholds (V_{IN_UVLO+} and $V_{IN\_UVLO\_HYS}$)

The PRM monitors the +IN terminal. It will not start until the input voltage exceeds the undervoltage recovery threshold (V_{IN_UVLO+}) and will shut down if the input voltage crosses below this threshold by more than the undervoltage lockout hysteresis ($V_{IN\_UVLO\_HYS}$). V_{IN_UVLO} will set byte 3, bit 3 in the MFR_STATUS_FAULTS (F0h) status register, as well as byte 2, bit 0 FLT_FALLING_EDGE.

Input Overvoltage Lockout and Recovery Thresholds (V_{IN_OVLO+} and $V_{IN\_OVLO\_HYS}$)

If the input voltage rises above the overvoltage lockout threshold (V_{IN_OVLO+}), the PRM will shut down. The PRM will attempt to recover once the input voltage has reduced below this threshold by at least the overvoltage lockout hysteresis ($V_{IN\_OVLO\_HYS}$). A V_{IN_OVLO} will set byte 3, bit 4 in the MFR_STATUS_FAULTS (F0h) status register, as well as byte 2, bit 0 FLT_FALLING_EDGE.

Overtemperature Fault Threshold (T_{OT})

The PRM features an overtemperature shut down, which is designed to protect against catastrophic failure due to excessive temperatures. The overtemperature shut down cannot be used to ensure the device stays within the recommended operating temperature range, because the overtemperature threshold T_{OT} engages at or above the maximum rated temperature. When overtemperature shut down occurs, the PRM stops processing power and $\overline{FLT}$ drives low. The PRM will restart after the temperature has decreased below T_{OT} by at least the overtemperature restart hysteresis, T_{OT_HYS}.

If the overtemperature fault threshold is exceeded, byte 1, bit 0 in the MFR_STATUS_FAULTS (F0h) status register will be set. Unlike other faults, the Overtemperature Fault will not set byte 2, bit 0 FLT_FALLING_EDGE due to how the overtemperature condition is sensed.

Output Undervoltage (V_{OUT_UVP})

When the PRM operates as a constant current source, the output voltage must decline in order to maintain the set current trim at higher load conditions. The PRM will shut down if the output voltage declines below the UVP threshold, V_{OUT_UVP}.

A V_{OUT_UVP} fault will set byte 1, bit 2 in the MFR_STATUS_FAULTS (F0h) status register as well as byte 2, bit 0 FLT_FALLING_EDGE.

Output Overvoltage Threshold (V_{OUT_OVP})

The PRM will shut down if the output voltage rises above the OVP threshold, V_{OUT_OVP}.

A V_{OUT_OVP} fault will set byte 3, bit 5 in the MFR_STATUS_FAULTS (F0h) status register as well as byte 2, bit 0 FLT_FALLING_EDGE.

Output Voltage Negative (V_{OUT_NEG})

When the PRM output voltage is higher than $V_{OUT\_NEG\_RE\text{-}ARM}$, the Output Voltage Negative fault is armed. Once armed, if the PRM output voltage becomes reverse-biased by more than V_{OUT_NEG}, it will shut down and stop processing power. It will also set byte 3, bit 6 in the MFR_STATUS_FAULTS (F0h) status register, as well as byte 2, bit 0 FLT_FALLING_EDGE.

This can occur if the module is disabled or shuts down due to another fault, and either the load is inductive and brings V_{OUT} below ground, or if the PRM output is connected to a downstream load such as a VTM™ which sinks current, which can generate a negative voltage bias on the PRM output terminal.

When the PRM is disabled via EN, or has shut down due to any fault type, the output voltage negative fault is blanked from further activation until the output voltage again exceeds $V_{OUT\_NEG\_RE\text{-}ARM}$. This permits the PRM to be easily restarted even when a negative V_{OUT} condition persists (as may be the case with a downstream current sink present, like an active VTM powertrain).

All fault flags, if set, will remain asserted until cleared by the host or once the PRM input power is removed.

EAIN High (EAIN_HI)

When operating multiple PRMs in an array, the EAO terminal is interconnected between units in order to facilitate accurate current sharing. If the output voltage trim setting is not identical among units then it is possible that the output voltage sensed by the error amplifier is too high for the compensation.

If the EAO amplifier reference voltage is 120% of the expected reference voltage, the unit will shut down and an EAIN_HI fault will occur.

An EAIN high fault will set byte 2, bit 5 in the MFR_STATUS_FAULTS (F0h) status register as well as byte 2, bit 0 FLT_FALLING_EDGE.

EAO Overload (V_{EAO_OL} and t_{EAO_OL})

EAO, the control input voltage to the internal modulator, is driven by the internal error amplifier closing the module control loop. The voltage on this terminal varies according to the input voltage, the output trim setting and the load condition.

In cases where the PRM cannot support a load at a given input voltage and trim setting and the voltage on the EAO terminal exceeds the specified EAO overload threshold (V_{EAO_OL}), the overload timer starts. If this condition persists for longer than t_{EAO_OL}, the $\overline{FLT}$ terminal is asserted low and the unit will shut down.

An EAO overload fault will set byte 2, bit 1 in the MFR_STATUS_FAULTS (F0h) status register as well as byte 2, bit 0 FLT_FALLING_EDGE.

$\overline{FLT}$ Fault

If the $\overline{FLT}$ terminal is pulled low, the unit will shut down in the same manner as other faults listed here. Byte 2, bit 0 FLT_FALLING_EDGE bit will be set in the MFR_STATUS_FAULTS (F0h) status register.

Thermal Design

Thermal management of PRM internal power dissipation is critical to reliable operation, and ample cooling is preferred since efficiency and reliability are better at lower internal temperatures. Figure 23 shows a thermal impedance model that can be used to estimate the maximum temperature of the hottest internal component for a given electrical and thermal operating condition.

The circuit model assumes each of those areas identified as thermal boundaries are isothermal although not necessarily the same temperature as the other boundary areas. Use of electrically insulating TIM (Thermal Interface Material) is required to prevent shorting conductive surfaces on the module case.

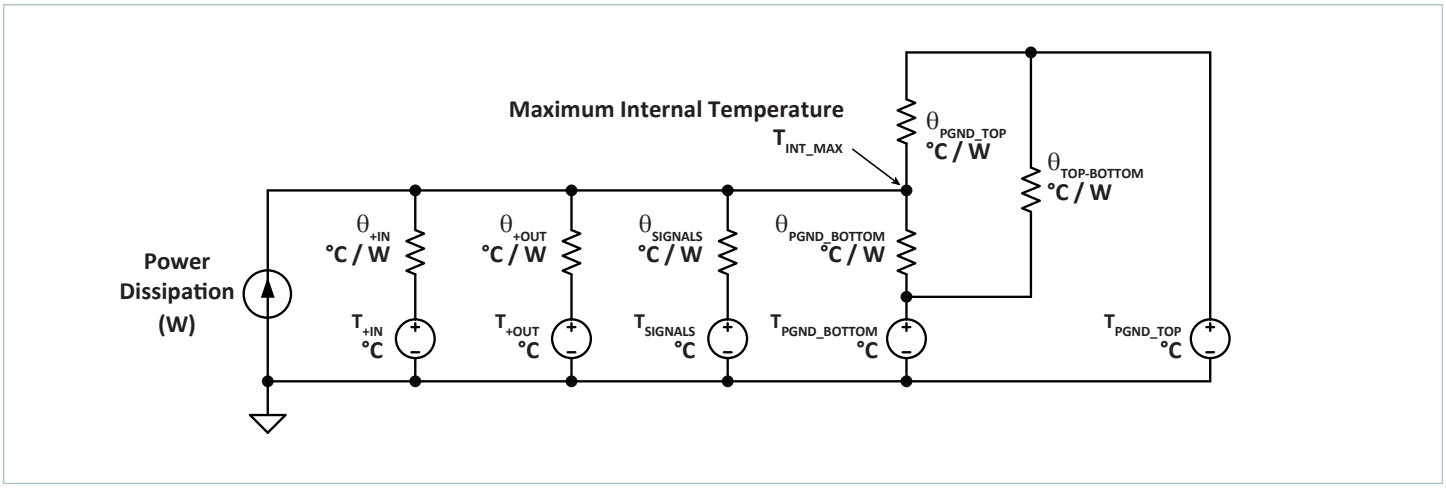


Figure 23 — *Thermal model*

Symbol	Thermal Impedance (°C / W)	Definition of Estimated Thermal Resistance
θ_{PGND_TOP}	0.99	From top of PGND terminal to maximum temperature internal component
θ_{+IN}	7.9	From +IN terminal to maximum temperature internal component
θ_{+OUT}	7.2	From +OUT terminal to maximum temperature internal component
$\theta_{SIGNALS}$	17	From collective signal terminals to maximum temperature internal component
θ_{PGND_BOTTOM}	1.1	From bottom of PGND terminal to maximum temperature internal component
θ_{TOP_BOTTOM}	14	Between top and bottom of PGND

Table 1 — *Preliminary thermal impedances*

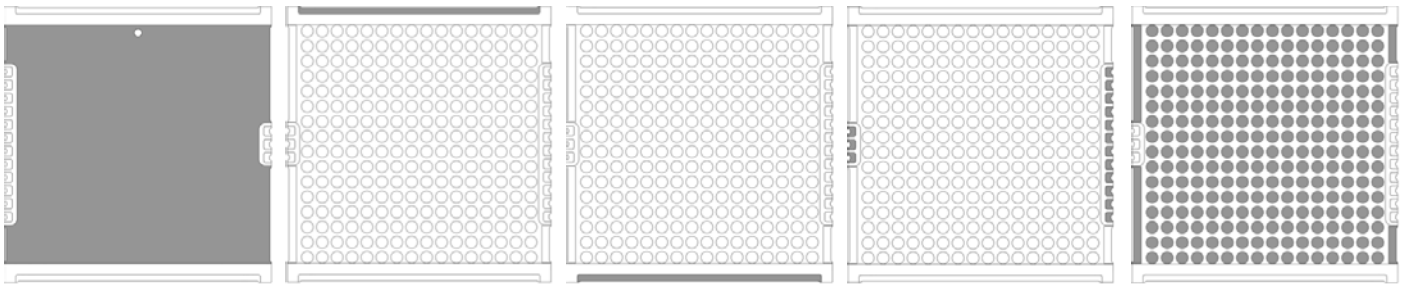


Figure 24 — *Thermal model boundary conditions; area defined as shaded*

Thermal Design — Typical Performance

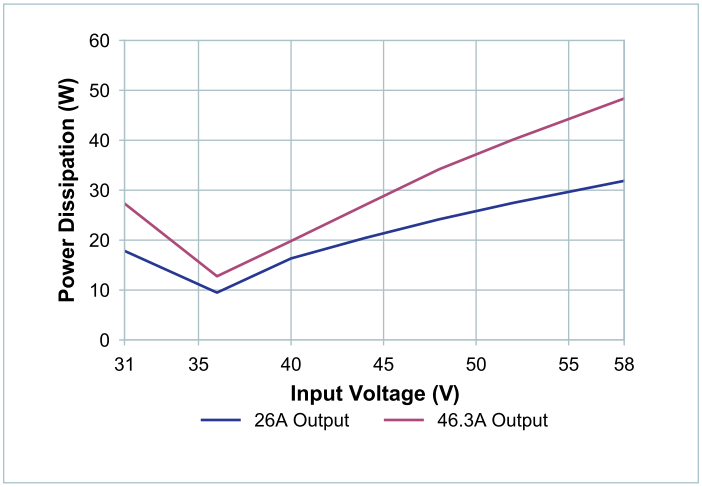


Figure 25 — *Power dissipation vs. line voltage, V_{OUT} = 36V, at 25°C case temperature*

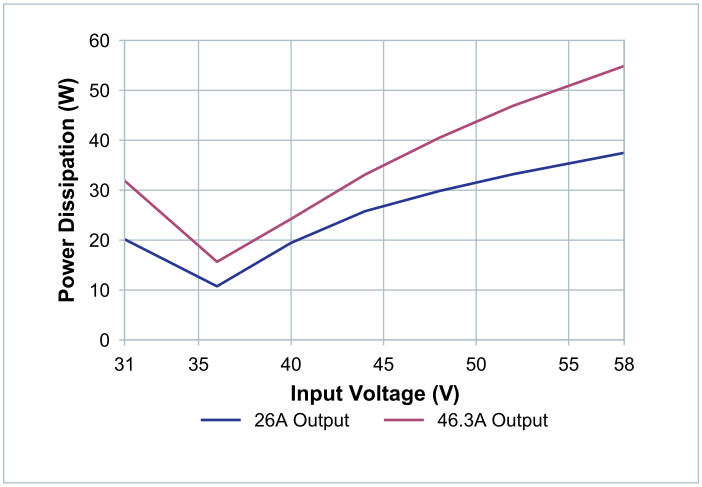


Figure 26 — *Power dissipation vs. line voltage, V_{OUT} = 36V, at 85°C case temperature*

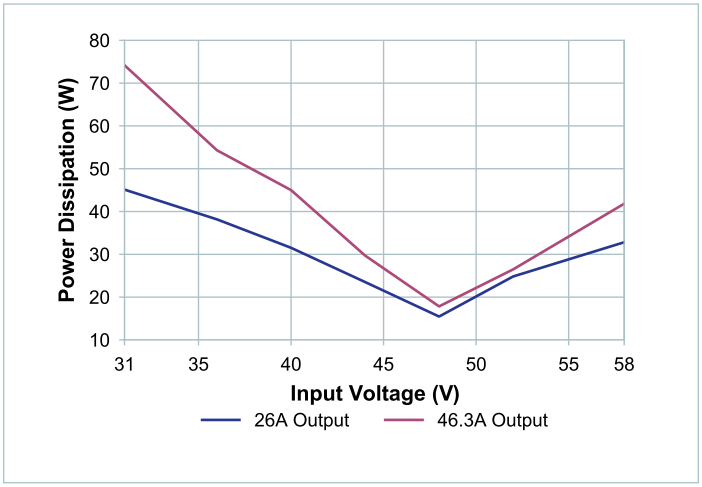


Figure 27 — *Power dissipation vs. line voltage, V_{OUT} = 48V, at 25°C case temperature*

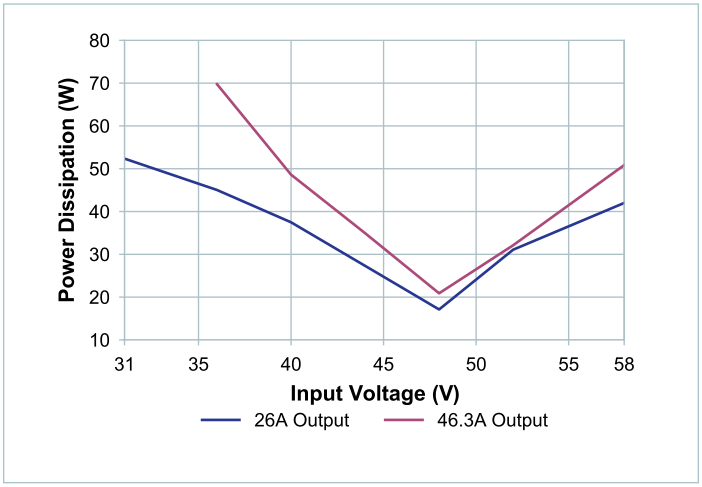


Figure 28 — *Power dissipation vs. line voltage, V_{OUT} = 48V, at 85°C case temperature*

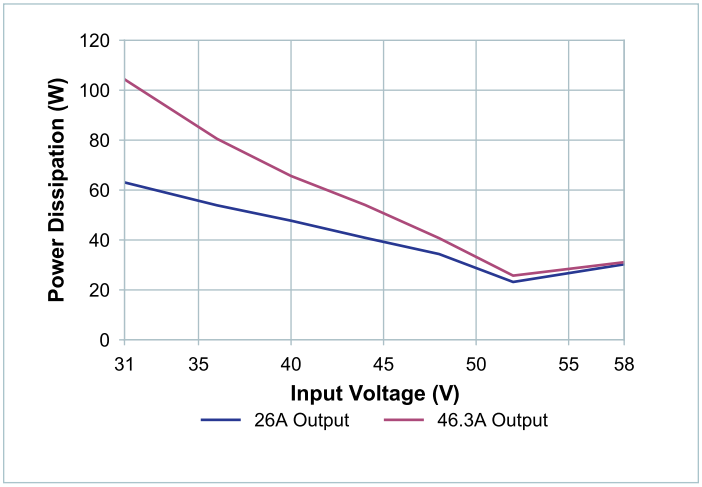


Figure 29 — *Power dissipation vs. line voltage, V_{OUT} = 54V, at 25°C case temperature*

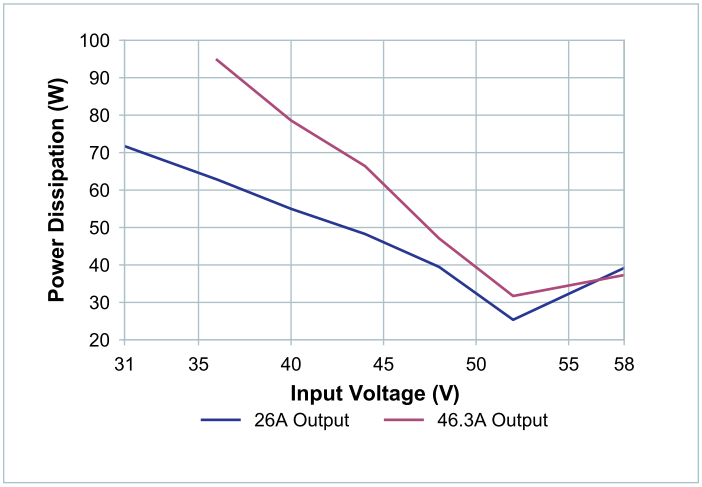


Figure 30 — *Power dissipation vs. line voltage, V_{OUT} = 54V, at 85°C case temperature*

PMBus Interface

Refer to "PMBus Power System Management Protocol Specification Revision 1.3, Part I and II" for complete PMBus® specifications details visit http://pmbus.org

The PRM is a PMBus child and will respond only to host commands listed in this sections. Dedicated address (ADDR), Clock (SCL) and data (SDA) terminals are available; the optional SMBALERT# signal is not supported.

Device Address

The PRM PMBus address can be set using a 1% resistor from the ADDR terminal to ground. The following table lists the available addresses and the corresponding resistor value to use.

The PRM does not support SMBus Address Resolution protocol. The address is set at initial power up and then remains fixed until power is removed.

Restricted Address

The PRM also responds to address 0x6A, but this address is for factory use only and cannot be used for any Supported Command in the list below. This address is fixed and cannot be change. Care must be taken that no other device on the bus uses address 0x6A in order to avoid address collisions.

7-bit Hex Address	Resistor Value, 1% (kΩ)
62h	0.0
63h	12.1
64h	20.0
65h	28.0
66h	35.7
67h	44.2
68h	52.3
69h	open

Supported Command List and Supported Commands Transaction Type

Command Name	Command Code	Function	Default Data Content	SMBus Write Transaction	SMBus Read Transaction	Number of Data Bytes	Data Format	PEC
OPERATION	01h	PMBus enable/disable	84h	Write Byte	Read Byte	1	bit	Supported
CLEAR_FAULTS	03h	Clear fault status register	n/a	Send Byte	n/a	0	bit	Unsupported
STORE_USER_CODE	17h	Writes variable parameter to non-volatile memory	n/a	Write Byte	n/a	1	bit	Unsupported
CAPABILITY	19h	PRM key capabilities set by factory	A0h	n/a	Read Byte	1	bit	Supported
VOUT_MODE	20h	Format for VOUT_COMMAND	17h	n/a	Read Byte	1	bit	Supported
VOUT_COMMAND	21h	Set PRM output voltage	6000h	Write Word	Read Word	2	ULINEAR16	Supported
VOUT_TRANSITION_RATE	27h	Set PRM output voltage slew rate in operation	1900h	Write Word	Read Word	2	LINEAR11	Supported
IOUT_OC_FAULT_LIMIT	46h	Set PRM constant current limit	E3F0h	Write Word	Read Word	2	LINEAR11	Supported
STATUS_BYTE	78h	Fault Readback	n/a	n/a	Read Byte	1	bit	Supported
STATUS_WORD	79h	Generic Fault Readback	n/a	n/a	Read Word	2	bit	Supported
READ_VIN	88h	PRM Input Voltage	n/a	n/a	Read Word	2	LINEAR11	Supported
READ_VOUT	8Bh	PRM Output Voltage	n/a	n/a	Read Word	2	ULINEAR16	Supported
READ_IOUT	8Ch	PRM Output Current	n/a	n/a	Read Word	2	LINEAR11	Supported
READ_TEMPERATURE_1	8Dh	PRM Temperature at Regulator Controller	n/a	n/a	Read Word	2	LINEAR11	Supported
MFR_ID	99h	Manufacturer ID	"VI"	n/a	Block Read	2	ASCII	Unsupported
IC_DEVICE_ID	ADh	Device identification	"4210008"	n/a	Block Read	7	ASCII	Unsupported
MFR_STATUS_FAULTS	F0h	PRM Specific Faults	n/a	n/a	READ 32	4	bit	Supported

PMBus Command Definitions

A summary of the PMBus commands supported by the PRM are described in the following sections.

OPERATION Command (01h)

The OPERATION command and the PRM EN terminal must both be active for the PRM to be enabled. Default value is 84h at ON stage, and can be set to 04h for OFF stage.

Note that the Host OPERATION command will not enable the PRM if the PRM EN terminal is disabled in hardware with respect to the preset terminal polarity. The OPERATION command provides ON/OFF control only with the PRM EN terminal active.

If synchronous start up is required in the system, it is recommended to use the command from Host PMBus or the PRM EN terminal in order to achieve simultaneous array start up.

CLEAR_FAULTS Command (03h)

This command clears all status bits that have been previously set. Persistent or active faults are re-asserted again once cleared, except for "$\overline{\text{FLT}}$ falling edge" bit, which is edge-triggered. All faults are latched once asserted in the PRM. Registered faults will not be cleared when the PRM powertrain is disabled through the $\overline{\text{FLT}}$ or EN terminal.

STORE_USER_CODE Command (17h)

STORE_USER_CODE can save the following command values to non-volatile memory. At subsequent power-ups, this stored value is used for the PRM.

For example, to store data of VOUT_COMMAND to non-volatile memory, the following transaction is sent: WRITE 0x17 0x21

STORE_USER_CODE can only be used NSTORE_USER_CODE times before all non-volatile memory is consumed.

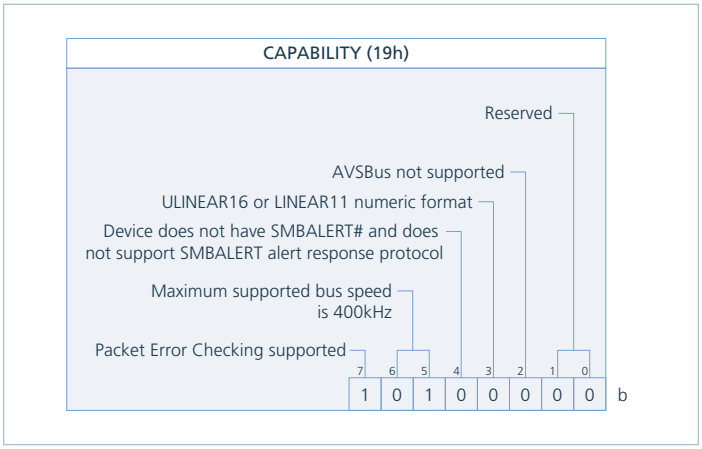
$N_{STORE\_USER\_CODE}$ = 8 (maximum)

Name	Code
OPERATION	0x01
VOUT_COMMAND	0x21
VOUT_TRANSITION_RATE	0x27
IOUT_OC_FAULT_LIMIT	0x46

CAPABILITY Command (19h)

The PRM returns a default value of A0h. This value indicates that the Packet Error Checking (PEC) is supported, PMBus® frequency is up to 400kHz, the SMBALERT# bit is not supported and that the numeric data can be LINEAR11 or ULINEAR16. See supported data command table indicating each command respective data reporting format.

Refer to the PMBus Power System Management Protocol Specification – Part II – Revision 1.3 for details on reported LINEAR11 and ULINEAR16 numeric format.



VOUT_MODE Command (20h)

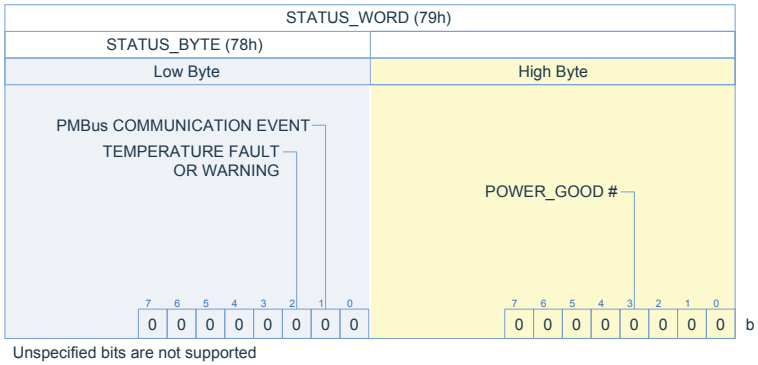
The PRM VOUT_MODE command is read-only. Set to a default value of 17h.

VOUT_COMMAND Command (21h)

VOUT_COMMAND causes the PRM to set the output voltage to the commanded value. Format is ULINEAR16 with –9 exponent, high byte, low byte. When multiple PRMs are used in parallel to create a high-power array, the group command protocol should be used when the VOUT_COMMAND is issued to change the output voltage. The group command protocol will cause all PRMs in the array to wait until the last unit receives the VOUT_COMMAND before collectively updating their output voltage setting. Not using the group command protocol can lead to nuisance detection of EAIN_HI faults for units which are programmed lower than the others in the array.

IOUT_OC_FAULT_LIMIT Command (46h)

The value of this register is set in both volatile and non-volatile memory. The value of the above-mentioned constant-current mode level is set by default to 63A (E3F0h). The limit level can be set up to other value. For example: In order for a limit to be set to 26A, one would send a write command with a (E1A0h) Data Word.



STATUS_BYTE (78h) and STATUS_WORD (79h)

Although the PRM powertrain will self-restart once fault conditions are cleared, all fault or warning flags, if set, will remain asserted until cleared by the host or once PRM input power is removed. This includes overtemperature warning and communication faults.

STATUS_WORD and STATUS_BYTE can be cleared by sending CLEAR_FAULTS (03h) command.

The TEMPERATURE FAULT bit reflects that an overtemperature shut down of PRM occurred.

The PMBus COMMUNICATION EVENT bit is set when a communication fault occurs. See the PMBus Communication Fault section for details.

The POWER_GOOD# bit is set any time the PRM is not in the enabled state to indicate that the powertrain is inactive and not switching. The POWER_GOOD# bit is cleared when the PRM is in the active and enabled state after the powertrain is active and soft-start has elapsed. The POWER_ GOOD# bit cannot be cleared as it always reflects the current state of the module.

READ_VIN Command (88h)

READ_VIN returns the input voltage telemetry in LINEAR11 format.

READ_VOUT Command (8Bh)

READ_VOUT returns the output voltage telemetry. As with the VOUT_COMMAND, the returned data format is ULINEAR16 with an exponent of –9.

READ_IOUT Command (8Ch)

READ_IOUT returns the output current telemetry in LINEAR11 format.

READ_TEMPERATURE_1 (8Dh)

READ_TEMPERATURE_1 returns the measured temperature at the powertrain controller. This temperature can be used as a relative gauge to the operating temperature of one internal area of the module.

READ_TEMPERATURE_1 is not sufficient to design or validate any module-level thermal solution. Thermal design must use the module power dissipation and thermal resistance model to ensure that all areas of the module internal circuitry are kept below the maximum operating temperature.

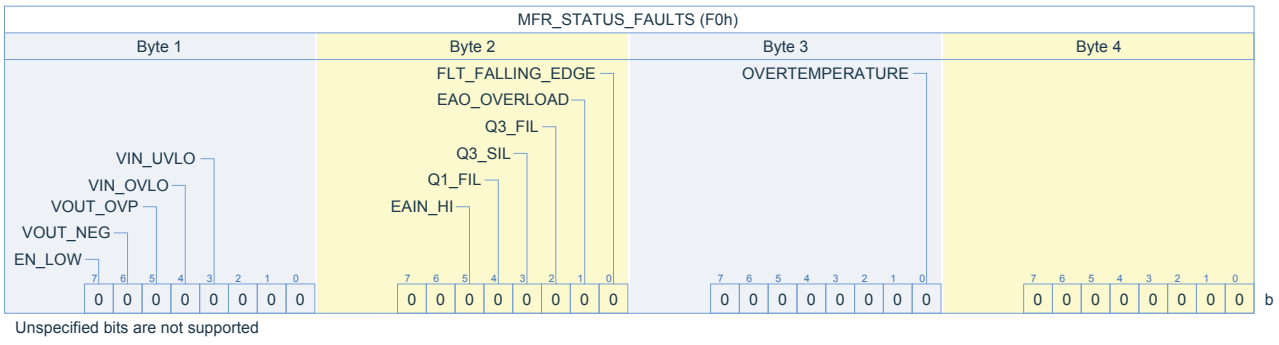
MFR_ID (99h)

This read-only command will return "VI" as two ASCII bytes, indicating the manufacturer Vicor Corporation.

MFR_STATUS_FAULTS (F0h)

This command returns four bytes; the first three are used and are defined below. All fault or warning flags, if set, will remain asserted until cleared by the host. A CLEAR_FAULTS (03h) command should be issued after power is initially applied to clear any fault flags which are set during module initialization.

Note: For information detailing detection and response to specific faults, see Functional Description section.



PMBus Communication Fault

Module Behavior

Corrupted data, unrecognized commands or other PMBus® protocol violations have no impact on powertrain functionality.

PMBus Reporting Characteristics

The below tables summarize data transmission and data content faults as implemented in the PRM.

Data Transmission Faults Implementation

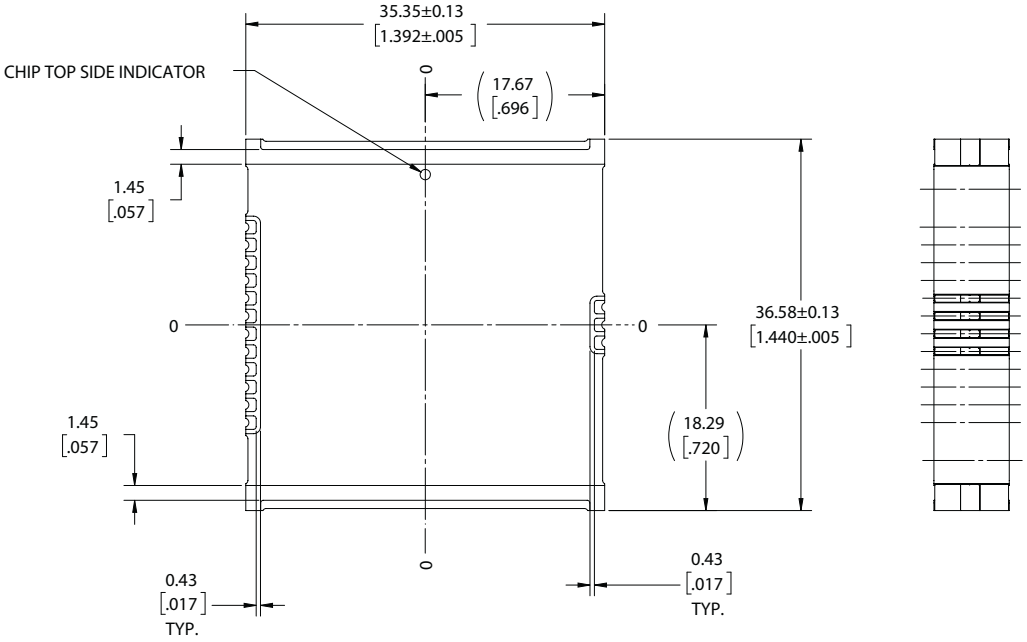
Section	Description	STATUS_BYTE	Notes
		CML	
10.8.1	Corrupted data	X	PEC failure
10.8.2	Sending too few bits		Device will ignore transmission
10.8.3	Reading too few bits		No response
10.8.4	Host sends or reads too few bytes	X	CML set on writes only
10.8.5	Host sends too many bytes	X	
10.8.6	Reading too many bytes		Read will report old data
10.8.7	Device busy		Clock stretch prior to ACK

Data Content Faults Implementation

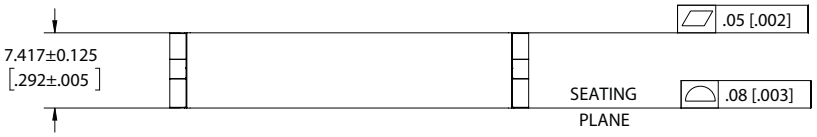
Section	Description	STATUS_BYTE	Notes
		CML	
10.9.1	Improperly set read bit in the address byte		Not interpreted as a fault; device will respond normally
10.9.2	Unsupported command code	X	
10.9.3	Invalid or unsupported data	X	
10.9.4	Data out of range		No response
10.9.5	Reserved bits		Not interpreted as a fault; no response

Package Drawing Top & Side View

PRM3735 TC3
(Reference DWG # 51312 Rev 2)



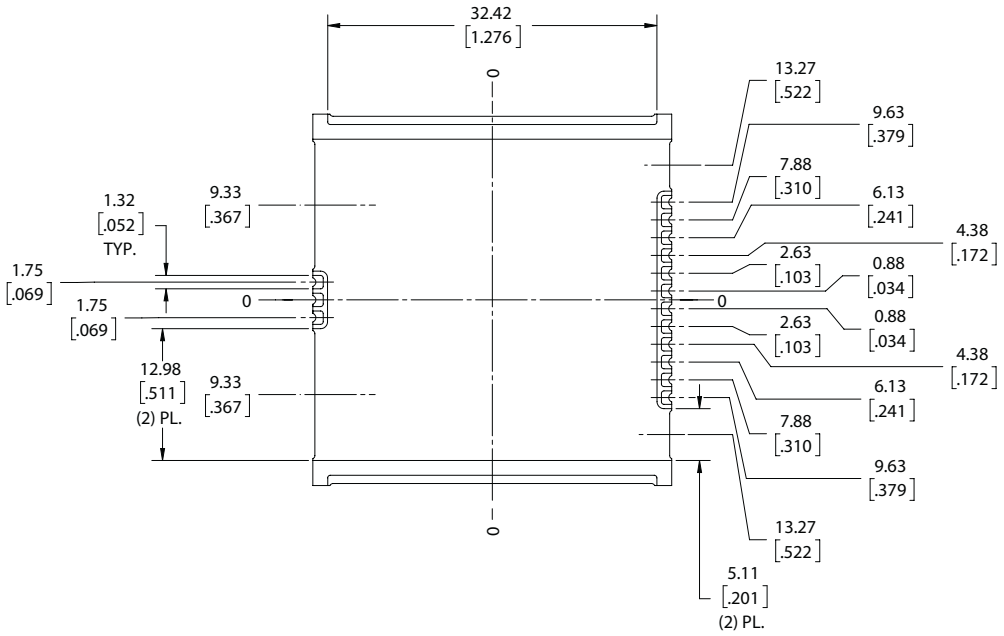
TOP VIEW
(COMPONENT SIDE)



NOTES:
1- UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE MM [INCH]
2- TOLERANCES ARE:
DECIMALS
X.X [X.XX] = ±0.25 [0.01]
X.XX [X.XXX] = ±0.127 [0.005]
ANGLES = ±1°

Package Drawing Bottom View

PRM3735 TC3
(Reference DWG # 51312 Rev 2)



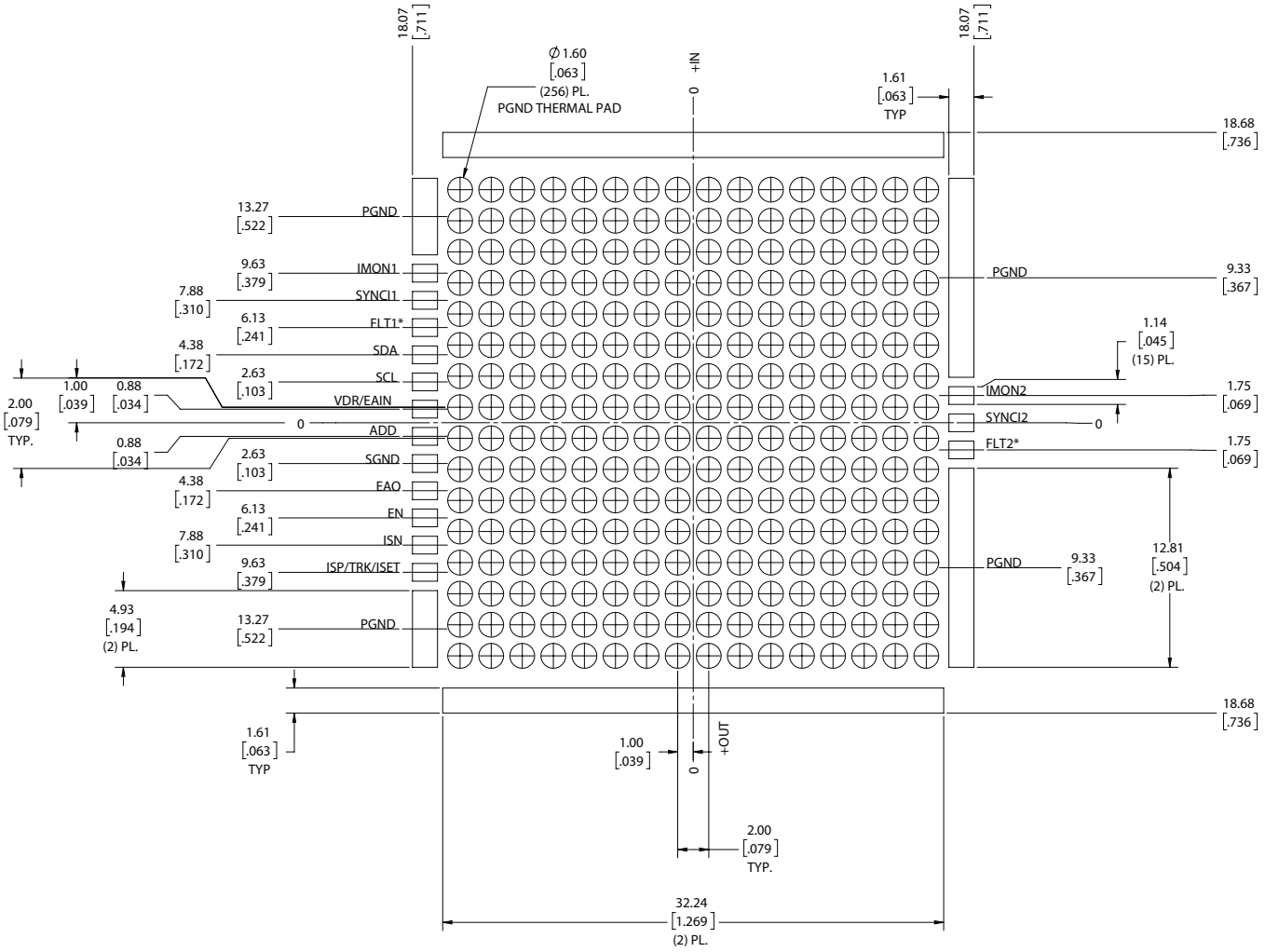
BOTTOM VIEW

Notes:

1. Dimensional origin defined by package center. See package drawing top view.

Recommended Land Pattern (Component Side)

PRM3735 TC3
(Reference DWG # 51312 Rev 2)

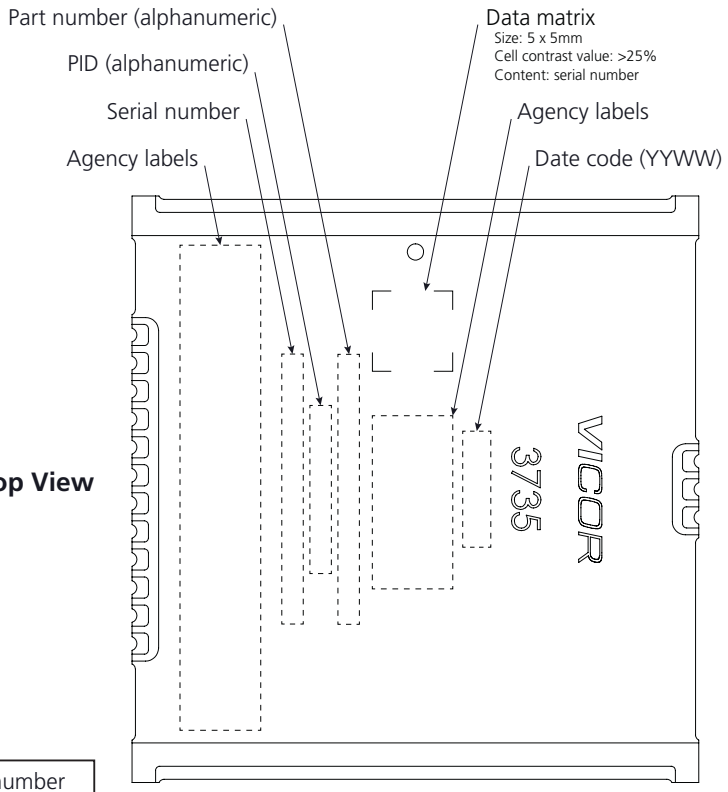


RECOMMENDED LAND PATTERN
(COMPONENT SIDE)

Notes:

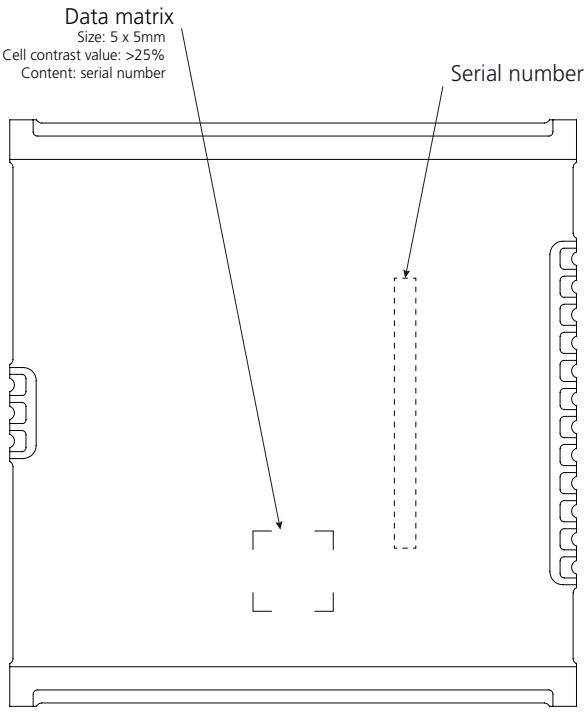
1. Dimensional origin defined by package center. See package drawing top view.

Package Marking Specification



Top View

Example 16-digit serial number
A 023 10 04 00004143
Year (2023)
Month (October)
Day (4th)
Module count (4143rd of this day)



Bottom View

Revision History

Revision	Date	Description	Page Number(s)
1.0	04/25/24	Initial release	n/a
1.1	06/24/24	Added array size specification, updated rated power and current notes Updated SCL, SDA specification Corrected SMBus write transaction for 01h, F0h Revised diagram formats for 19h, 78h, 79h, F0h	6 9 19 20, 21
1.2	07/30/24	Updated outline drawings	23, 24, 25
1.3	10/07/24	Updated features and benefits	1

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Contact Us: https://www.vicorpower.com/contact-us

Vicor Corporation
25 Frontage Road
Andover, MA, USA 01810
Tel: 800-735-6200
Fax: 978-475-6715
www.vicorpower.com

email
Customer Service: custserv@vicorpower.com
Technical Support: apps@vicorpower.com