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Paper 13
Date: May 24, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

DELTA ELECTRONICS, INC.,
Petitioner,

v.

VICOR CORP.,
Patent Owner.

IPR2024-00227
Patent 9,516,761 B2

Before GEORGIANNA W. BRADEN, KARA L. SZPONDOWSKI, and SEAN P. O'HANLON, *Administrative Patent Judges*.

O'HANLON, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

Granting Patent Owner's Motion to Seal
37 C.F.R. § 42.14

I. INTRODUCTION

A. Background

Delta Electronics, Inc. ("Petitioner") filed a Petition for *inter partes* review of claims 1–7 ("the challenged claims") of U.S. Patent No. 9,516,761 B2 (Ex. 1001, "the '761 patent"). Paper 1 ("Pet."), 5. Vicor Corp. ("Patent Owner") filed a Preliminary Response. Paper 9 ("Prelim. Resp."). [1]

Institution of an *inter partes* review is authorized by statute only when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). We have authority, acting on the designation of the Director, to determine whether to institute an *inter partes* review. 37 C.F.R. § 42.4(a). For the reasons set forth below, upon considering the Petition, Preliminary Response, and evidence of record, we conclude that the information presented in the Petition fails to establish a reasonable likelihood that Petitioner would prevail in showing the unpatentability of any of the challenged claims. Accordingly, we decline to institute *inter partes* review.

B. Real Parties in Interest

Petitioner identifies itself, Delta Electronics (Americas), Ltd., Delta Electronics (USA), Inc., Cyntec Co., Ltd., Delta Electronics (Thailand) Public Company Limited, and DET Logistics (USA) Corporation as real

[1] A publicly available version of the Preliminary Response was filed as Paper 11.

parties in interest. Pet. 95. In addition, Petitioner states that the following entities are not real parties in interest, but Petitioner is disclosing them for purposes of transparency: Hon Hai Precision Industry Co. Ltd., Foxconn Industrial Internet Co. Ltd., FII USA Inc., Ingrasys Technology Inc., Ingrasys Technology USA Inc., Quanta Computer, Inc., Quanta Computer USA Inc., Quanta Cloud Technology, Inc., Quanta Cloud Technology USA, LLC, and QCH, Inc. *Id.* at n.12.

Patent Owner identifies itself as the sole real party in interest. Paper 7, 1.

C. Related Matters

The parties indicate that the '761 patent is the subject of the following district court proceeding:

> *Vicor Corp. v. Delta Electronics, Inc.*, No. 2-23-cv-00323 (E.D. Tex. filed July 12, 2023).

Pet. 96; Paper 7, 1. Petitioner asserts that this proceeding has been stayed. Pet. 96.

The parties indicate that the '761 patent is the subject of the following International Trade Commission proceeding:

> *Certain Power Converter Modules and Computing Systems Containing the Same*, No. 337-TA-1370 (filed July 12, 2023).

Pet. 96; Paper 7, 1.

D. The Challenged Patent

The '761 patent is titled "Encapsulated Modular Power Converter with Symmetric Heat Distribution" and relates to "[a] method of encapsulating a panel of electronic components such as power converters

[that] reduces wasted printed circuit board area." Ex. 1001, codes (54), (57). An encapsulated electronic power converter module "may comprise a printed circuit assembly over-molded with an encapsulant to form some or all of the package and exterior structure or surfaces of the module." *Id.* at 1:30–34. According to the '761 patent, "[e]ncapsulation in this manner may aid in conducting heat out of the over-molded components, i.e., components that are mounted on the printed circuit assembly and covered with encapsulant." *Id.* at 1:34–37.

Figure 27 of the '761 patent is reproduced below.

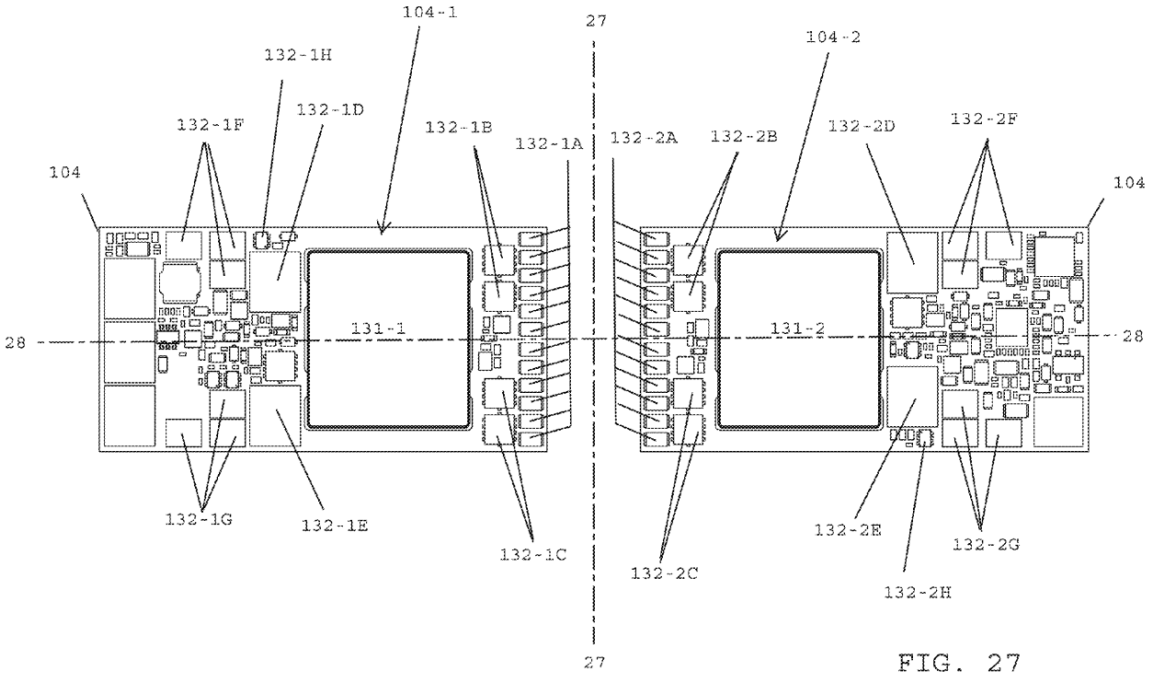


FIG. 27

Figure 27 shows plan views of top 104-2 and bottom 104-1 of printed circuit board ("PCB") 104 illustrating symmetry of component layouts, such as input field-effect transistors ("FETs") 132-2D, 132-2E. 132-1D, 132-1E and output FETs 132-2B, 132-2C, 132-1B, 132-1C. Ex. 1001, 10:37–38, 23:27–38. "The populated PCB 104 is shown rotated along the vertical

axis 27 in FIG. 27 to show the symmetry of the components." *Id.* at 23:21–23.

> The components may be arranged between the PCB surfaces according to heat dissipated during operation. For example, the heat dissipative components may be arranged in a manner that distributes the heat evenly between the two PCB surfaces allowing heat produced by power dissipating devices to be extracted from both surfaces of the PCB improving the thermal performance.

Id. at 24:47–53. As illustrated in Figure 27, "the significant power dissipative components of the input cells are arranged to have one component of one cell mounted on one surface with the respective component from the other cell mounted on the other surface." *Id.* at 25:4–8. "[T]he FETs are arranged such that during operation, the power FETs on the top surface dissipate power at a level that is comparable to the level of power dissipated by the power FETs on the bottom surface." *Id.* at 25:11–15. The '761 patent describes several benefits to this arrangement of power dissipative components, including decreased stress, enhanced thermal performance, enhanced co-planarity and structural integrity, reduced conduction losses, and increased efficiency. *Id.* at 23:38–42, 25:25–32.

E. The Challenged Claims

Petitioner challenges claims 1–7 of the '761 patent. Pet. 6. Claim 1 is the sole independent claim and is reproduced below with Petitioner's identifiers in bold.

1. An apparatus comprising:

1[a] a power converter including

1[b] a printed circuit board ("PCB") comprising a plurality of conductive layers and having a top surface and a bottom surface;

1[c] a magnetic core structure magnetically coupled to a winding formed by traces in one or more of the conductive layers in the PCB; and

1[d] a plurality of power semiconductor devices, a first set of the power semiconductor devices being mounted on the top surface and electrically connected to dissipate power at a level, Pt, during operation of the converter, a second set of the power semiconductor devices being mounted on the bottom surface and electrically connected to dissipate power at a level, Pb, during operation of the converter;

1[e] wherein the power semiconductor devices are distributed between the first and second sets to distribute heat generation during operation of the converter such that each level Pt, Pb is less than 150% of the other level Pb, Pt.

Ex. 1001, 28:13–33.

F. Asserted Challenges to Patentability

The Petition relies on the following prior art references:

Name	Reference	Exhibit
Ericsson-BMR	Ericsson AB, "Technical Specification BMR 453 series DC/DC converters, Input 36-75 V, Output up to 60 A/396 W" (July 2010)	1007
Wanes	US 6,965,517 B2, issued November 15, 2005	1009
Takeshima	US 6,970,367 B2, issued November 29, 2005	1010
Spiazzi	G. Spiazzi et al., *Layout Considerations and Thermal Analysis of a 1.8 MHz Resonant VRM*, Conference Record - IAS Annual Meeting (IEEE Industry Applications Society), 1993–2000 (2007)	1011

Name	Reference	Exhibit
BMR-2008	Ericsson AB, "Technical Specification BMR 453 DC/DC Converters, Input 36-75 V, Output 33 A/400 W" (Sept. 2008)	1026

Petitioner asserts the following challenges to patentability:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–5, 7	103(a)[2]	Ericsson-BMR
1–5, 7	103(a)	BMR-2008
1–5, 7	103(a)	Ericsson-BMR, Spiazzi
1–5, 7	103(a)	BMR-2008, Spiazzi
1–7	103(a)	Ericsson-BMR, Wanes
1–7	103(a)	BMR-2008, Wanes
1–7	103(a)	Takeshima
1–7	103(a)	Takeshima, Spiazzi
1–7	103(a)	Takeshima, Wanes
1–7	103(a)	Ericsson-BMR, Takeshima
1–7	103(a)	BMR-2008, Takeshima
1–7	103(a)	Spiazzi, Wanes

Pet. 6. Petitioner submits a declaration of Steven B. Leeb, Ph.D. (Ex. 1002, "Leeb Declaration") in support of its contentions. Patent Owner submits a declaration of Juan Rivas-Davila, Ph.D. (Ex. 2001) in support of its contentions.

[2] The application resulting in the '761 patent claims priority to a date prior to the date when the Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112–29, 125 Stat. 284 (2011), took effect. Thus, we refer to the pre-AIA version of section 103.

II. PATENTABILITY ANALYSIS

A. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) when in evidence, any objective evidence of nonobviousness.[3] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

The level of ordinary skill in the art is "a prism or lens" through which we view the prior art and the claimed invention. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). The person of ordinary skill in the art is a hypothetical person presumed to have known the relevant art at the time of the invention. *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). In determining the level of ordinary skill in the art, we may consider certain factors, including: "(1) the educational level of the inventor; (2) type of

[3] The parties present arguments regarding objective indicia of non-obviousness. Pet. 94; Prelim. Resp. 69–75. Because we determine that the Petition is deficient for other reasons as set forth herein, we do not address these arguments.

problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field." *Best Med. Int'l, Inc. v. Elekta Inc.*, 46 F.4th 1346, 1353 (Fed. Cir. 2022) (quoting *Daiichi Sankyo Co. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007)). "The patent's purpose can also be informative." *Id.*

Petitioner contends that a person having ordinary skill in the art at the time of the invention would have had "at least a Master's degree in electrical engineering and two or more years of work experience relating to power electronics and the manufacture of power converters or printed circuit board design for power converters," but acknowledges that "[a]dditional education might compensate for less work experience, and vice-versa." Pet. 14 (citing Ex. 1013, 79).

Patent Owner does not contest Petitioner's proposed definition or proffer a definition of its own. *See generally* Prelim. Resp. Patent Owner's witness, Dr. Rivas-Davila, asserts that he applies Petitioner's definition. Ex. 2001 ¶ 77.

We find Petitioner's definition of the level of ordinary skill in the art to be consistent with the problems and solutions disclosed in the '761 patent and prior art of record, and adopt it as our own for purposes of this Decision. *See Okajima*, 261 F.3d at 1355.

C. Claim Construction

In an *inter partes* review, claims are construed using the same claim construction standard that would be used to construe the claims in a civil action under 35 U.S.C. § 282(b), including construing the claims in

accordance with the ordinary and customary meaning of such claims as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. 37 C.F.R. § 42.100(b). "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention" and "after reading the entire patent." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313, 1321 (Fed. Cir. 2005) (en banc). In addition to the specification and prosecution history, we also consider use of the terms in other claims and extrinsic evidence including expert and inventor testimony, dictionaries, and learned treatises, although extrinsic evidence is less significant than the intrinsic record. *Id.* at 1312–17. Usually, the specification is dispositive, and it is the single best guide to the meaning of a disputed term. *Id.* at 1315.

"The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'" *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (alteration in original) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

1. Petitioner's Asserted Interpretations

Petitioner asserts that it "applies Patent Owner's apparent understanding of the terms as reflected in its infringement contentions, to the extent that Petitioner can understand Patent Owner's deficient and opaque contentions." Pet. 6–7 (citing Ex. 1025).

Petitioner does not identify which of the definitions of "terms as reflected in [Patent Owner's] infringement contentions" it asserts that we

should adopt. Notably, Petitioner does not cite to Exhibit 1025 in its mappings of the asserted references to the challenged claims. *See generally* Pet. Nor does Petitioner explain why we should adopt definitions that it characterizes as "deficient and opaque." *Id.* at 6–7. As such, Petitioner does not proffer any definitions for any claim terms.

2. Patent Owner's Asserted Interpretations

Patent Owner asserts that we should interpret limitation 1[d] "to require that 'the first and second sets of the power semiconductor devices comprise the complete set of power semiconductor devices in the power converter.'" Prelim. Resp. 18 (quoting Ex. 2001 ¶ 79); *see also id.* at 26–27 (asserting that we should interpret limitation 1[d] to require that "the first and second sets include[e] all power semiconductor devices of the power converter"). Patent Owner argues that "in a converter with a multiplicity of power semiconductor devices, the claim cannot be interpreted to arbitrarily include, or exclude, any *subset* of these power semiconductor devices." *Id.* at 22 (citing Ex. 2001 ¶¶ 85–87; *Apple Inc. v. Samsung Elecs. Co.*, 695 F.3d 1370, 1379 (Fed. Cir. 2013)). Patent Owner argues that the'761 patent supports its interpretation by, according to Patent Owner, "focus[ing] on balancing the overall heat generation from all power [Metal Oxide Semiconductor Field Effect Transistors ('MOSFETS')]." *Id.* at 23 (quoting Ex. 1001, 25:11–24) (citing Ex. 2001 ¶ 85).

Petitioner does not proffer an explicit interpretation of this claim language. *See generally* Pet. Nor did Petitioner seek authorization to submit additional briefing to address Patent Owner's interpretation of this claim language.

The '761 patent discloses symmetrical distribution of components between PCB surfaces.[4] Ex. 1001, 23:24–42, 24:7–25:32. The '761 patent explains that this applies to both input and output components:

> Many of the larger components may be distributed equally between both faces of PCB 104 as shown in FIG. 27. For example, the *four input field effect transistors* (FETs) 132-2D, 132-2E, 132-1D, 132-1E are shown equally distributed between the top 104-2 and bottom 104-1 surfaces with two FETs on each surface. Similar equal distribution between the top 104-2 and bottom 104-1 surfaces of the PCB 104 are shown for the *eight output FETs* 132-2B, 132-2C, 132-1B, 132-1C with four output FETs on each surface; the *twelve input capacitors*, 132-2F, 132-2G, 132-1F, 132-1G, with six input capacitors on each surface; and twenty *four output capacitors* 132-2A, 132-1A with twelve output capacitors on each surface.

Id. at 23:25–37 (emphases added). The '761 patent states that this arrangement distributes heat-generating components evenly between the two PCB surfaces:

> The components may be arranged between the PCB surfaces according to heat dissipated during operation. For example, the heat dissipative components may be arranged in a manner that distributes the heat evenly between the two PCB surfaces allowing heat produced by power dissipating devices to be extracted from both surfaces of the PCB improving the thermal performance.

Id. at 24:47–53. The '761 patent identifies FETs as heat-generating components and, as an example, explains that input FETs 132-1D, 132-1E are positioned on the PCB bottom surface and input FETs 132-2D, 132-2E are positioned on the PCB top surface. *Id.* at 24:53–25:4, Fig. 27. That is,

[4] The distribution of power semiconductor devices was not discussed during prosecution of the application that resulted in the '761 patent. *See generally* Ex. 1004.

"[t]o ensure heat dissipation symmetry between the two surfaces, the cells may be arranged in mirror image layouts" such that "the significant power dissipative components of the input cells are arranged to have one component of one cell mounted on one surface with the respective component from the other cell mounted on the other surface." *Id.* at 24:65–25:8. The '761 patent explains that "the FETs are arranged such that during operation, the power FETs on the top surface dissipate power at a level that is comparable to the level of power dissipated by the power FETs on the bottom surface." *Id.* at 25:11–15. The '761 patent purports that the benefits of such symmetrical placement of power dissipative components on the PCB top and bottom surfaces provides several benefits, including decreased stress, enhanced thermal performance, enhanced co-planarity and structural integrity, reduced conduction losses, and increased efficiency. *Id.* at 23:38–42, 25:25–32.

Thus, the '761 patent supports Patent Owner's asserted interpretation that the first and second sets include all of the power semiconductor devices of the power converter.

Our reviewing court interpreted similar claim language in *Apple*. Claim 6 was at issue in *Apple* and recited "[a]n apparatus for locating information in a network, comprising . . . a plurality of heuristic modules . . . wherein: each heuristic module corresponds to a respective area of search and employs a different, predetermined heuristic algorithm corresponding to said respective area." *Apple*, 695 F.3d at 1373. Apple argued:

> [C]laim 6 requires "a plurality" (just one) in which every module has a different heuristic algorithm (compared to the other modules within that plurality). Accordingly, as long as there is one such "one plurality"—i.e., at least two modules

> with different heuristic algorithms—the key limitation is satisfied. As to any remaining modules, Apple points out that claim 6 uses the open-ended term "comprising" in listing the limitations and concludes that the addition of other modules does not defeat a showing of infringement.

Id. at 1379.

The Federal Circuit disagreed with Apple's interpretation of "plurality." *Apple*, 695 F.3d at 1379. The court stated:

> Apple's argument essentially urges us to hold that "plurality" refers not to all but a subset of modules. As we pointed out, however, the district court has construed "plurality" to mean "at least two," without any indication that the term refers to a hand-picked selection of a larger set. Nor do the parties seem to disagree with that construction, at least at this stage. Accordingly, despite the use of "comprising," claim 6 is not amenable to the addition of other modules that do not use different heuristic algorithms because such addition would impermissibly wipe out the express limitation that requires every module to have a unique heuristic algorithm.

Id.

Similarly to the claim at issue in *Apple*, claim 1 of the '761 patent recites:

> [a]n apparatus comprising: a power converter including . . . a plurality of power semiconductor devices, a first set of the power semiconductor devices being mounted on the [PCB] top surface . . . , a second set of the power semiconductor devices being mounted on the [PCB] bottom surface . . . wherein the power semiconductor devices are distributed between the first and second sets.

Ex. 1001, 28:13–33. The court's analysis of "plurality" in *Apple* applies here. Consistent with *Apple* and other precedent of our reviewing court, we interpret "plurality" to mean two or more. *See Dayco Prods., Inc. v. Total Containment, Inc.*, 258 F.3d 1317, 1327–28 (Fed. Cir. 2001) ("In accordance

with standard dictionary definitions, we have held that 'plurality,' when used in a claim, refers to two or more items, absent some indication to the contrary."); *York Prods., Inc. v. Cent. Tractor Farm & Family Ctr.*, 99 F.3d 1568, 1575 (Fed. Cir. 1996) ("The term ['plurality'] means, simply, 'the state of being plural.'"). And as explained above, neither the '761 patent nor its prosecution history indicates that "a plurality of power semiconductor devices" as used in claim 1 refers to a subset, rather than all, of the power semiconductor devices in the power converter. *See* Ex. 1001, 23:24–42, 24:7–25:32; *generally*, Ex. 1004.

As discussed in more detail below, Petitioner maps "plurality of power semiconductor devices" to a subset of the power semiconductor devices in the device disclosed in Ericsson-BMR, implicitly interpreting this language to mean less than all of the power converter power semiconductor devices of the power converter. Petitioner's interpretation that "plurality of power semiconductor devices" is satisfied by a subset of the power semiconductor devices does not accord with the Federal Circuit's interpretation of "plurality" as set forth in *Apple* and is at odds with the requirement that "the power semiconductor devices are distributed between the first and second sets" as recited in claim 1. *See Apple*, 695 F.3d at 1379.

Accordingly, we interpret "a power converter including . . . a plurality of power semiconductor devices" as recited in claim 1 to refer to all of the power semiconductor devices in the power converter, not merely a subset of the power semiconductor devices.

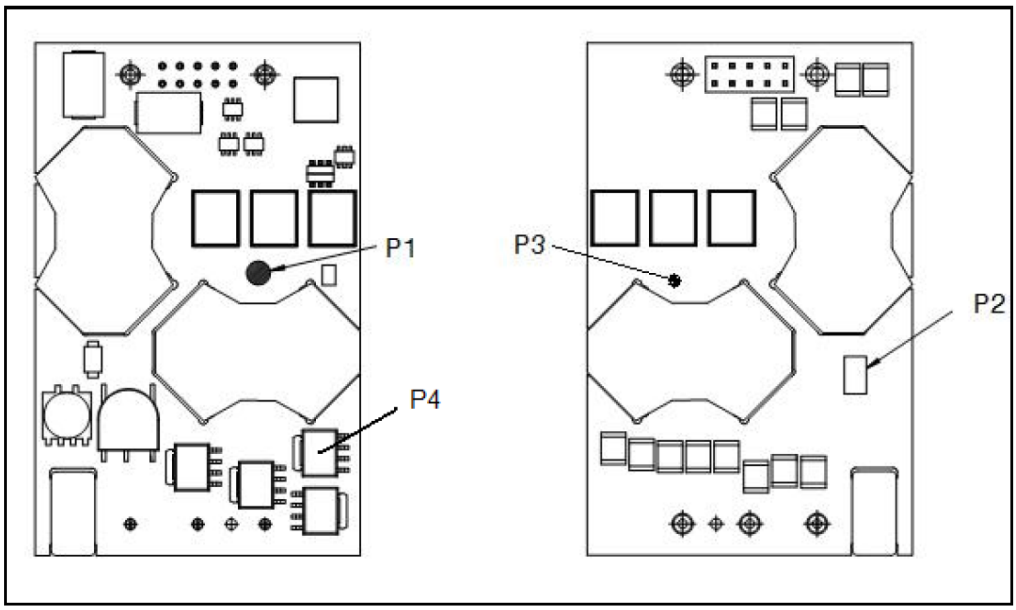
D. Overview of the Asserted Prior Art

1. Ericsson-BMR (Exhibit 1007)

Ericsson-BMR is a technical specification for Ericsson's BMR 453 series DC/DC converter shown in the picture on its cover page, which is reproduced below.

Ex. 1007, 1. The picture reproduced above appears to be overlapping top and bottom views of a DC-DC power converter.

In a section titled "Thermal Consideration," Ericsson-BMR states that "[f]or products mounted on a [Printed Wiring Board] without a heatsink attached, cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is [dependent] on the airflow across the product." Ex. 1007, 24. Ericsson-BMR shows top and bottom views of the converter, which are reproduced below, and indicates that the best airflow direction is from right to left. *Id.*



The figure reproduced above is an illustration showing the top and bottom view of the DC-DC converter, showing outlines of the circuit components. *Id.*

2. Wanes (Exhibit 1009)

Wanes relates to "devices and methods of assembly relating to components for printed circuit boards ('PCBs')." Ex. 1009, 1:9–11. Wanes notes that, "for a power converter PCB, power conversion components in the circuit generate significant amounts of heat, which must be properly dissipated." *Id.* at 1:20–23. Figures 9A and 9B of Wanes are reproduced below.

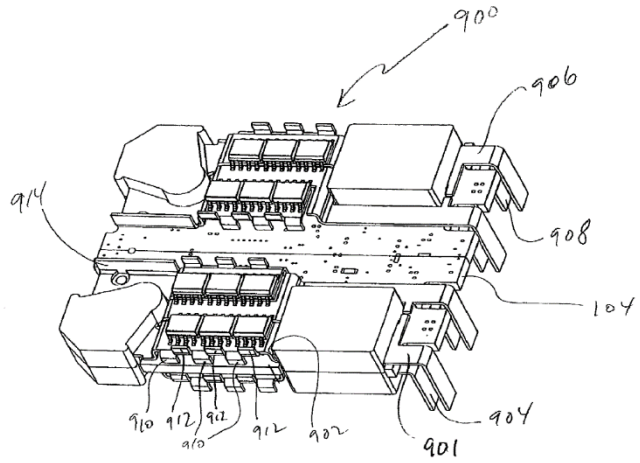


Figure 9A

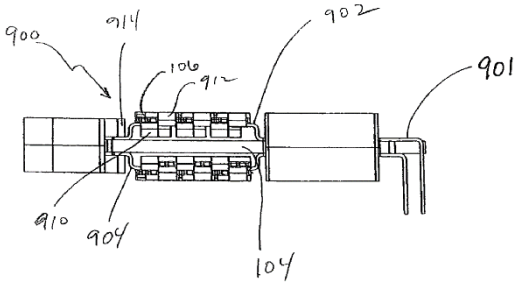


FIGURE 9B

Figures 9A and 9B are illustrations showing perspective and side views, respectively, of an assembly of power converter 900, including substrates 901, 904, 906, 908 mounted to a side of PCB 104. *Id.* at 3:32–35, 11:4–13. "Substrate 901 has an offset or raised section 902 that, when mounted to PCB 104, is spaced from PCB 104." *Id.* at 11:7–9.

3. Takeshima (Exhibit 1010)

Takeshima "relates to a switching power supply device installed in the interior of electronic equipment." Ex. 1010, 1:6–7. Takeshima purports that "[i]n recent years, the tendency in the conditions of electric power supply to [central processing units] incorporated in electronic equipment including information devices such as personal computers, and communication devices such as mobile telephones, has been toward lower voltage and higher current." *Id.* at 2:7–11. Takeshima states that its "object is to provide a high efficiency and small-sized switching power supply device that is capable of supplying a direct current at low voltage and high current and at a constant voltage irrespective of the power consumption of load." *Id.* at 3:7–12.

Figures 1 and 2 of Takeshima are reproduced below.

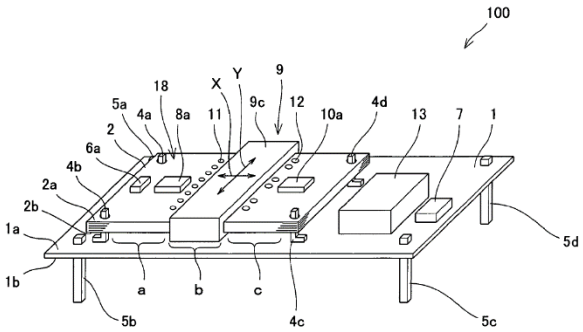


Fig. 1

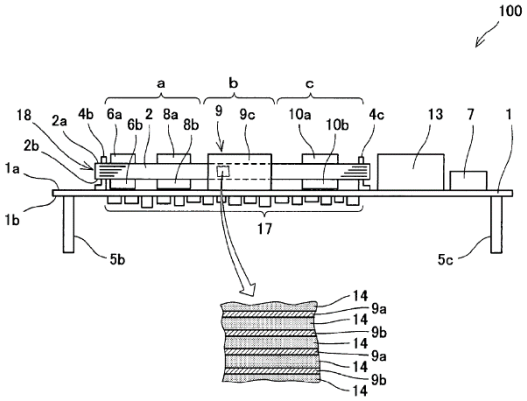


Fig. 2

Figures 1 and 2 are illustrations showing oblique and side views, respectively, of switching power supply device 100. Ex. 1010, 9:23–27. The switching power supply device is "configured so that a multi-layer printed circuit board 2 having connecting terminals 4a to 4d, the inductance 13, the output smoothing capacitor 7, and the control circuit 17 are arranged at predetermined positions on a main printed circuit board 1 having connecting terminals 5a to 5d." *Id*. at 9:38–44. "MOSFETs 8a and 8b and the input smoothing capacitors 6a and 6b are mounted on a first major surface 2a and a second major surface 2b of the multi-layer printed circuit board 2 within the primary-side inverter region a," and "the first diode 10a and second diode 10b are mounted on the first major surface 2a and the second major surface 2b of the multi-layer printed circuit board 2 within the secondary-side rectification region c." *Id*. at 10:51–55, 10:60–63. Takeshima explains that an inverter circuit is formed when "[t]he input smoothing capacitors 6a and 6b, the MOSFETs 8a and 8b, and the transformer primary winding 9a of the transformer 9 are electrically connected by a plurality of wiring lines . . . formed on the multi-layer printed

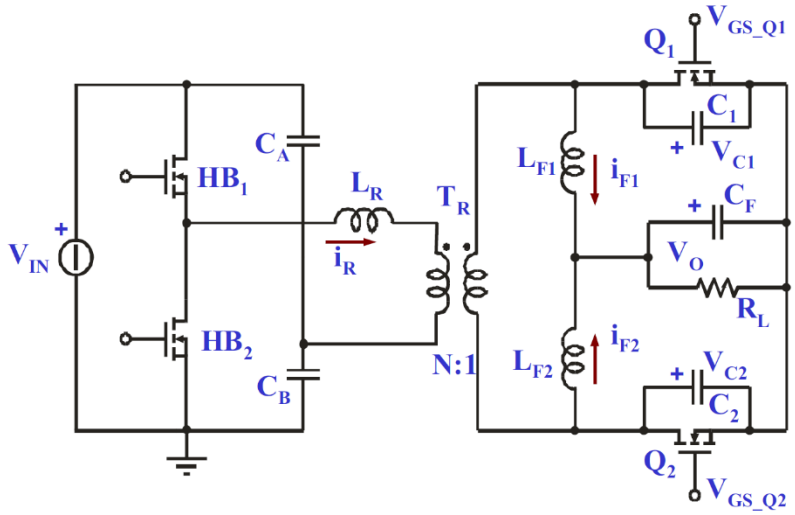
circuit board 2," and a rectifier circuit is formed when "the first diode 10a, the second diode 10b, and the transformer secondary winding 9b of the transformer 9 are electrically connected by a plurality of wiring lines . . . formed on the multi-layer printed circuit board 2." *Id*. at 10:67–11:12.

4. Spiazzi (Exhibit 1011)

Spiazzi relates to "[h]igh frequency dc-dc converters for Voltage Regulator Module (VRM) applications." Ex. 1011, 1.[5] Spiazzi purports that "[p]ractical realization of modern high current and high switching frequency converters . . . requires a good control on layout-dependent parasitic components and on the power losses (thermal management), in order to meet the goal of high efficiency and reliability." *Id*. According to Spiazzi, "component placement and routing have a strong impact not only on parasitic components, but also on the overall converter efficiency, thus affecting the thermal management." *Id*. Spiazzi considers "the techniques for removing the produced heat from the components in order to keep them at a reasonable maximum temperature" to be a "crucial issue." *Id*. at 3.

Spiazzi discusses layout and thermal issues relating to a 1.8 MHz VRM. Ex. 1011, 1. Figure 1(a) of Spiazzi is reproduced below.

[5] Our citations are to the exhibit pagination added by Petitioner, as are Patent Owner's. *See, e.g.*, Prelim. Resp. 39 (citing Ex. 1011, 3). Petitioner, however, cites to the original pagination rather than the exhibit pagination. *See, e.g.*, Pet. 36 (citing Ex. 1011, 1993–94).



a)

Figure 1(a) is a circuit diagram showing the schematics of the half-bridge resonant VRM. *Id.* at 2. Figure 5 of Spiazzi is reproduced below.[6]

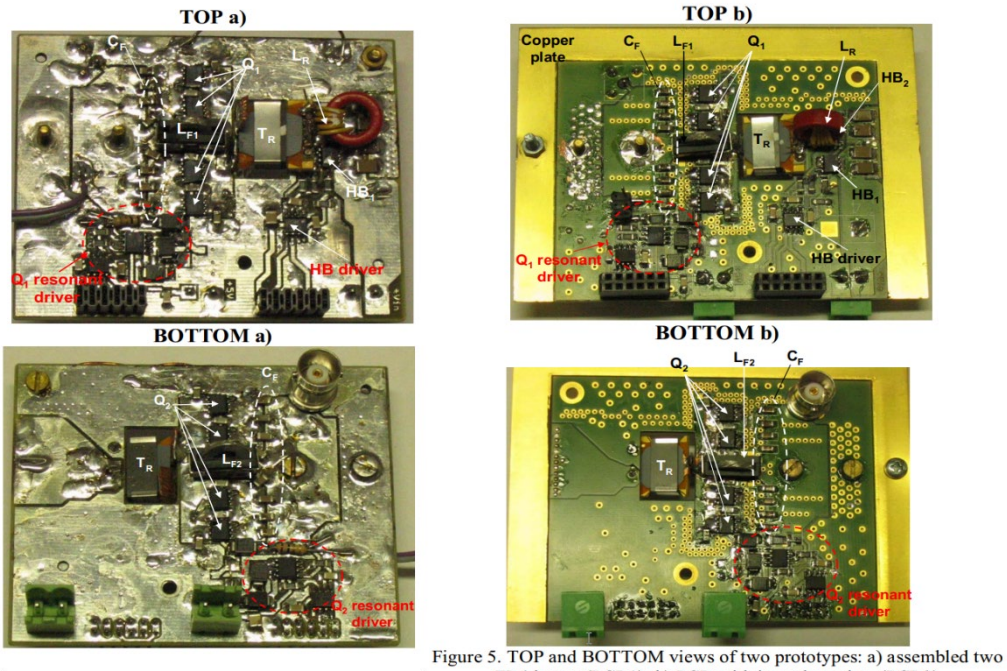


Figure 5. TOP and BOTTOM views of two prototypes: a) assembled two FR4 layers (PCB1); b) PCB with inner baseplate (PCB2)

[6] Spiazzi presents the four pictures arranged vertically in a column. Ex. 1011, 4. We have modified the figure to present the top and bottom pictures of each prototype in separate columns.

Figure 5 includes photographs of top and bottom views of two prototype layouts,

> one using two layers of standard FR4 PCB (0.8 mm thickness) joined together to form an equivalent three layer PCB (see Fig. 5a) with an equivalent total inner layer thickness of 0.14 mm (PCB1), and the other built assembling two epoxy layers (0.5 mm thickness) on both sides of 0.7 mm thick copper baseplate shown in Fig. 5b (PCB2).

Id. at 3. Figure 11 of Spiazzi is reproduced below.

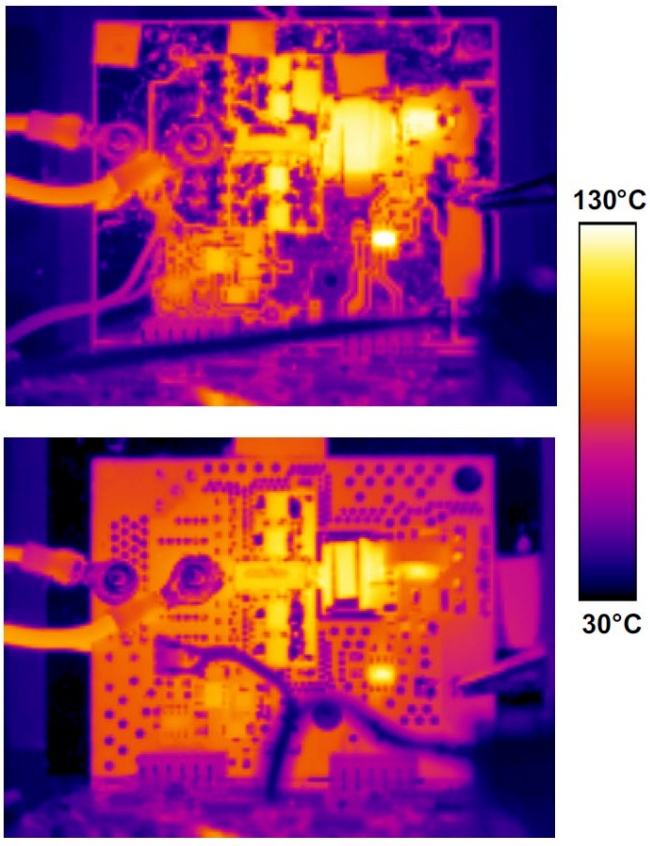


Figure 11. Thermal map of the up-side of the converter measured with the IR camera for the two solutions (top: PCB1; bottom: PCB2) with 50 A load current.

Figure 11 includes pictures showing "the thermal map of the upside of the converter measured with the IR camera for the two solutions (top: PCB1; down: PCB2) with 50 A of load current." *Id.* at 7. According to Spiazzi,

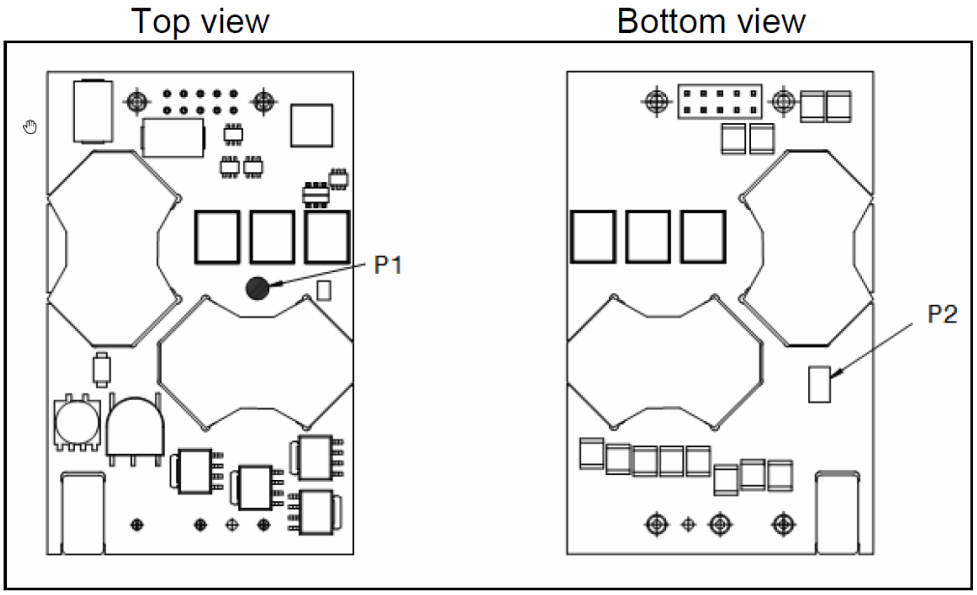
"[s]imilar results were obtained for the downward surfaces." *Id.* Spiazzi reports that the solution with integrated baseplate (PCB2) shows better a thermal behavior: "better thermal distribution over the board, a lower peak temperature of active and passive components and a lower mean temperature on the board." *Id.*

5. BMR-2008 (Exhibit 1026)

BMR-2008 is a technical specification for Ericsson's BMR 453 DC/DC converter shown in the picture on its cover page, which is reproduced below.

Ex. 1026, 1. The picture reproduced above appears to be overlapping top and bottom views of a DC-DC power converter.

In a section titled "Thermal Consideration," BMR-2008 states that "[c]ooling is achieved mainly by conduction, from the pins to the host board, and convection, which is [dependent] on the airflow across the converter." Ex. 1026, 15. BMR-2008 shows top and bottom views of the converter, which are reproduced below.



The figure reproduced above is an illustration showing the top and bottom view of the DC-DC converter, showing outlines of the circuit components. *Id.*

E. Asserted Obviousness Based on Ericsson-BMR

Petitioner argues that claims 1–5 and 7 would have been obvious in view of Ericsson-BMR. Pet. 14–34. In support of its showing, Petitioner relies upon the Leeb Declaration. *Id.* (citing Ex. 1002). We have reviewed Petitioner's assertions and supporting evidence. For the reasons discussed below, and based on the record before us, we determine that Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that at least one challenged claim would have been obvious in view of Ericsson-BMR.

1. Petitioner's Reliance on the Product Disclosed in Ericsson-BMR

Petitioner maps disclosure in Ericsson-BMR to each of the recitations of independent claim 1. Pet. 14–27. However, Petitioner relies on other

references it asserts to describe the same product described in Ericsson-BMR. *See id.* at 17–18 (citing Ex. 1014), 20–21 (citing Ex. 1014; Ex. 1018, "visual inspection," and undefined "additional documentary evidence").

Patent Owner argues that this challenge to the '761 patent claims "may be non-statutory because it likely relates to a product, not a printed publication." Prelim. Resp. 28. Patent Owner notes that, in addition to Ericsson-BMR, Petitioner relies on Exhibits 1014 and 1018 and argues that Petitioner's reliance on these additional descriptions of the Ericsson product is improper because "[Petitioner] provides no evidence that these documents relate to the same product variation . . . or the same release dates, such that each document is describing something with identical features," instead Petitioner "simply *assumes* that any product literature naturally describes the same product." *Id.* at 29–31. Continuing, Patent Owner argues that "if [Petitioner] is relying on an underlying product, then the Ground does not comply with 35 U.S.C. §311(b)." *Id.* at 31.

To the extent Petitioner relies on the other references to provide additional information regarding the *product* described in Ericsson-BMR, such reliance on a product is inappropriate for an *inter partes* review, which must be based only on patents and printed publications. 35 U.S.C. § 311(b) ("A petitioner in an inter partes review may request to cancel as unpatentable 1 or more claims of a patent only on a ground that could be raised under section 102 or 103 and *only on the basis of prior art consisting of patents or printed publications*." (emphasis added)). To the extent Petitioner argues that the *product* described in the referenced documents renders the challenged claims obvious, we decline to consider such improper

arguments. Rather, we will consider Petitioner's arguments based solely on the disclosures of the referenced documents.

2. Petitioner's Challenge

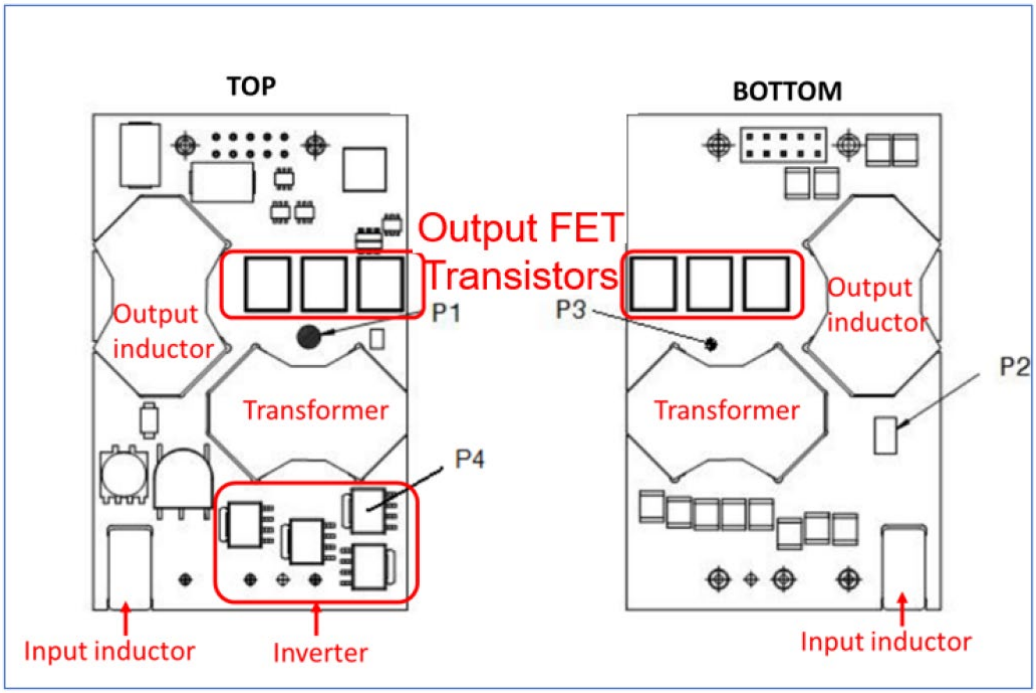
Independent claim 1 recites, in relevant part,

> a power converter including . . . a plurality of power semiconductor devices, a first set of the power semiconductor devices being mounted on the [PCB] top surface . . . , a second set of the power semiconductor devices being mounted on the [PCB] bottom surface . . . wherein the power semiconductor devices are distributed between the first and second sets.

Ex. 1001, 28:13–33. Petitioner asserts that Ericsson-BMR discloses six output FETs, which Petitioner maps to the recited plurality of power semiconductor devices. Pet. 21–22 (citing Ex. 1007, 1, 24; Ex. 1002 ¶¶ 60–74) (reproducing and annotating a figure from Ericsson-BMR page 24); *see also id.* at 24 (reproducing and annotating differently the figure from Ericsson-BMR page 24 (the "second annotated figure")).

Patent Owner argues that "the Petition focuses only on a *subset* of power semiconductor devices, namely the output (secondary-side) MOSFETs, while ignoring *input* MOSFETs." Prelim. Resp. 33 (reproducing Petitioner's second annotated figure). Patent Owner argues that the four components in this figure identified by Petitioner as the inverter (*see* Pet. 24) are four primary MOSFETs, which are power semiconductor devices. Prelim. Resp. 33–35 (citing Ex. 1007, 1, 24; Ex. 2001 ¶¶ 92–93; Pet. 23–24).

We agree with Patent Owner. We reproduce below Petitioner's second annotated figure.



Ericsson-BMR's figure (reproduced above) is an illustration depicting top and bottom views of a DC-DC converter product, and Petitioner has annotated the figure to identify the depicted components. Ex. 1007, 24; Pet. 24. Petitioner identifies four components in the lower right of the top view as an inverter. Pet. 24. Ericsson-BMR discloses that these components are primary MOSFETs. Ex. 1007, 24. Notably, there are no corresponding primary MOSFETs on the bottom view. *Id.* Although Petitioner argues that the "output FETs are power semiconductor devices," Petitioner omits the input MOSFETs from its mapping. *See* Pet. 22 (annotating the figure from Ericsson-BMR page 24).

As interpreted above, the recited plurality of power semiconductor devices refers to all of the power semiconductor devices in the power converter. By omitting the primary MOSFETs, Petitioner's mapping of Ericsson-BMR to this recitation is deficient. Petitioner fails to set forth a reasonable likelihood of prevailing on this challenge for this reason alone.

Independent claim 1 also recites "wherein the power semiconductor devices are distributed between the first and second sets to distribute heat generation during operation of the converter such that each level Pt, Pb is less than 150% of the other level Pb, Pt." Ex. 1001, 28:29–33. Petitioner argues that an ordinarily skilled artisan "would have known, or at least found obvious, that the current and voltage (and thus, power) through the top three power semiconductor devices would be equal (or at least approximately equal) over time to the bottom three power semiconductor devices." Pet. 25 (citing Ex. 1002 ¶ 76).

Patent Owner argues that, by ignoring the four primary MOSFETs, the Petition fails to meet this limitation. Prelim. Resp. 35. According to Patent Owner, "[b]ecause the heat generation of power semiconductor devices relates to power processed, [the seven] top-side MOSFETs process three times as much power [than the three bottom-side MOSFETs], giving rise to a commensurately greater amount of heat." *Id.* at 36 (citing Ex. 2001 ¶ 95).

We agree with Patent Owner. As noted above, the device disclosed in Ericsson-BMR includes four primary MOSFETs on the top surface in addition to the three secondary MOSFETs. *See* Ex. 1007, 24; Pet. 24. We are persuaded by the testimony of Patent Owners' witness, Dr. Rivas-Davila, who testifies that the MOSFETs on the top surface of the Ericsson-BMR device dissipate power at a level that is three times that of the MOSFETs on the bottom surface and therefore generate much more heat:

> [P]rimary switches process all of the converter's power, as do secondary switches. That is, if the amount of power processed by the converter is "P", primary switches process power P, and secondary switches process power P. Assuming, as [Petitioner]

> appears to assert, that the three secondary MOSFETs on the top side of the device process the same power as the three secondary MOSFETs on the bottom side of the device (each processing P/2), then the MOSFETs on the top side of the device process P+P/2 (or 1.5 P) and the MOSFETs on the bottom side of the device process 0.5 P, or three times less power. As the heat generation of power semiconductor devices relates to power processed, top-side MOSFETs process three times as much power, giving rise to a commensurately greater amount of heat.

Ex. 2001 ¶ 95.

For at least the foregoing reasons, Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that claim 1, or its dependent claims 2–5 and 7, would have been obvious in view of Ericsson-BMR.

F. Asserted Obviousness Based on Ericsson-BMR and Spiazzi

Petitioner argues that claims 1–5 and 7 would have been obvious in view of Ericsson-BMR and Spiazzi. Pet. 35–39. In support of its showing, Petitioner relies upon the Leeb Declaration. *Id.* (citing Ex. 1002). We have reviewed Petitioner's assertions and supporting evidence. For the reasons discussed below, and based on the record before us, we determine that Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that at least one challenged claim would have been obvious in view of the combination of Ericsson-BMR and Spiazzi.

Petitioner relies on Ericsson-BMR to disclose most of the recitations of independent claim 1 as set forth in the challenge based on Ericsson-BMR alone, and relies on Spiazzi to provide further teaching of Ericsson-BMR's semiconductors. Pet. 35–39. Regarding limitation 1[d], Petitioner relies on Spiazzi to teach "that Ericsson-BMR's components are power

semiconductor devices on the top and bottom surfaces and act as output switches." *Id.* at 36 (citing Ex. 1011, 1993–94, Fig. 1a). Petitioner argues that Spiazzi teaches "overlapping placement of the four MOSFET power semiconductor devices comprising the Q_1 output switch with the four MOSFET power semiconductor devices comprising Q_2." *Id.* (citing Ex. 1011, Fig. 5). Petitioner argues that an ordinarily skilled artisan "would . . . have found it obvious that the two sets of three components on the top and bottom of [Ericsson-BMR's] PCB were power semiconductor MOSFETs that comprised two output switches." *Id.* at 38.

Regarding limitation 1[e], Petitioner argues that "Spiazzi further confirms that Ericsson-BMR's full-bridge circuit would produce substantially similar results of power dissipation on both sides of the Ericsson-BMR module." Pet. 38. Petitioner argues that "Spiazzi teaches a half-bridge converter, which, like Ericsson-BMR's full-bridge converter, would have at least obviously applied balanced power cycles in order to avoid saturating the transformer." *Id.* (citing Ex. 1002 ¶ 112; Ex. 1011, Fig. 1a). Petitioner argues that Spiazzi's converter exhibits similar thermal mapping on both sides of its PCB, and that "Ericsson-BMR, under similar cycling, would also have featured power dissipation levels Pt and Pb that would at least be 'similar' and well within 150% of each other." *Id.* at 38–39 (citing Ex. 1011, 1999–2000).

Patent Owner contests this challenge for a number of reasons. Prelim. Resp. 37–46. First, Patent Owner argues that the Petition does not propose to modify Ericsson-BMR with the teachings of Spiazzi, so this challenge fails for the same reasons set forth for the challenge based on Ericsson-BMR alone. *Id.* at 37.

We agree with Patent Owner. Petitioner relies on Spiazzi to support its assertion "that Ericsson-BMR's components are power semiconductor devices on the top and bottom surfaces and act as output switches" and to "confirm[] that Ericsson-BMR's full-bridge circuit would produce substantially similar results of power dissipation on both sides of the Ericsson-BMR module." Pet. 36, 38. Petitioner does not rely on Spiazzi in any manner that would remedy the shortcomings noted above regarding Petitioner's reliance on Ericsson-BMR.

Next, Patent Owner argues that Petitioner's suggestion that Ericsson-BMR would achieve test results similar to those of Spiazzi is incorrect because "Spiazzi and [Ericsson-BMR] are very different circuits, with very different principles of operation." Prelim. Resp. 37–38 (citing Pet. 36–38; Ex. 2001 ¶ 101). Patent Owner argues that there are several differences between the devices disclosed by the two references, including different frequencies, whether voltage is regulated, and operation. *Id.* at 38–39 (citing Ex. 1011, 1, 3; Ex. 1007, 7; Ex. 1012, 1; Ex. 2001 ¶¶ 101–103; Pet. 38, 87). Patent Owner argues that Petitioner and Dr. Leeb's rationale for relying on the teachings Spiazzi, namely to apply "balanced power cycles in order to avoid saturating the transformer," is incorrect and contradicted by Dr. Leeb's testimony in another proceeding. *Id.* at 39–43 (quoting Pet. 38) (citing Ex. 1001, 2, Fig. 1a; Ex. 1002 ¶ 112; Ex. 1008, 148–50; Ex. 2001 ¶¶ 105–109; Ex. 2008, 116–17, Fig. 4.20B; Ex. 2009 ¶¶ 28, 31). In conclusion, Patent Owner argues:

> Because of the different nature of the Spiazzi and Ericsson BMR circuits, the fact that Spiazzi teaches that losses from its circuit are highly layout-dependent, and the fact that the Petition's only argument to connect the two circuits is

> factually wrong, the Petition has not shown that [an ordinarily skilled artisan] would have believed that testing on Spiazzi's converter would apply to Ericsson BMR.

Id. at 43 (citing Ex. 2001 ¶ 109).

Patent Owner persuasively refutes Petitioner's rationale for applying the teachings of Spiazzi to the device disclosed in Ericsson-BMR. As summarized above, Patent Owner identifies several differences between the circuits disclosed by Ericsson-BMR and Spiazzi that are unaddressed in the Petition. *See* Prelim. Resp. 37–41. Petitioner acknowledges that Spiazzi's disclosure describes a different type of circuit ("a half-bridge converter") than does Ericsson-BMR (a "full-bridge circuit"), but does not explain adequately why Spiazzi's asserted thermal mapping would apply to the different circuit of Ericsson-BMR. *See* Pet. 38. Nor does Petitioner explain adequately why modifying the operation of the device of Ericsson-BMR would have been obvious to an ordinarily skilled artisan, instead merely stating that the device disclosed in Ericsson-BMR should be operated with "similar cycling" as Spiazzi's device. *Id.*

Next, Patent Owner argues that "Spiazzi . . . places its input MOSFETs (HB1 and HB2) only on the top side of the device," which "unbalances heat generation of the power semiconductor devices." Prelim. Resp. 43 (citing Ex. 1011, Fig. 5a; Ex. 2001 ¶ 110). Patent Owner argues that, at best, Spiazzi discloses that its bottom-side MOSFETs dissipate power at a rate that is "more than three times less" than the top-side MOSFETs. *Id.* at 43–44 (citing Ex. 1011, 1996 (Table II); Ex. 2001 ¶¶ 110–111). Patent Owner argues that Spiazzi's statement that "[s]imilar results were obtained for the downward surfaces" cannot refer to all of the heating components listed in Table III because "numerous components in

Table III (such as primary MOSFETs 1 and 2, Primary driver, Primary inductor wound, Primary inductor core, and Transformer) are not found on the downward surface." *Id.* at 45 (citing Ex. 2001 ¶ 113).

We are persuaded that Petitioner's analysis of Spiazzi's teachings is, at best, incomplete. For example, as correctly noted by Patent Owner, Spiazzi's tested prototype PCBs include primary MOSFETs HB_1, HB_2 only on the top side of the PCB with no corresponding components on the bottom side. Ex. 1011, Fig. 5. As also correctly noted by Patent Owner, Spiazzi discloses that the primary MOSFETs dissipate more power than the secondary MOSFETs. *Id.* at 1996 (Table II). The Petition does not account for these heat-generating components on the top surface of Spiazzi's PCB. *See* Pet. 35–39.

Additionally, we are persuaded that the testimony of Petitioner's witness, Dr. Leeb, in this proceeding regarding saturation of half-bridge rectifiers appears to be at odds with his prior testimony. *See* Prelim. Resp. 41–43 (citing Ex. 2009 ¶ 31 (Dr. Leeb testifying in a district court proceeding that "[t]he topology of the PKM4303NF, a half-bridge topology, is one that is configured not to drive the transformer into saturation."); Ex. 2001 ¶ 107. Accordingly, we accord Dr. Leeb's testimony little weight.

For at least the foregoing reasons, Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that claim 1, or its dependent claims 2–5 and 7, would have been obvious in view of the combination of Ericsson-BMR and Spiazzi.

G. Asserted Obviousness Based on Ericsson-BMR and Wanes

Petitioner argues that claims 1–7 would have been obvious in view of Ericsson-BMR and Wanes. Pet. 40–53. In support of its showing, Petitioner relies upon the Leeb Declaration. *Id.* (citing Ex. 1002). We have reviewed Petitioner's assertions and supporting evidence. For the reasons discussed below, and based on the record before us, we determine that Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that at least one challenged claim would have been obvious in view of the combination of Ericsson-BMR and Wanes.

Petitioner relies on Ericsson-BMR to disclose most of the recitations of independent claim 1 as set forth in the challenge based on Ericsson-BMR alone, and relies on Wanes to provide further teaching of the composition of PCB layers and forming a winding by traces in PCB conductive layers. Pet. 40–42. Petitioner relies solely on the arguments advanced regarding the challenge based on Ericsson-BMR alone regarding limitations 1[d] and 1[e]. *Id.* at 42.

Petitioner's reliance on Wanes does not address or remedy the shortcomings in its reliance on Ericsson-BMR as discussed above. *See* Prelim. Resp. 47. Therefore, for at least the reasons set forth above, Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that claim 1, or its dependent claims 2–7, would have been obvious in view of the combination of Ericsson-BMR and Wanes.

H. Asserted Obviousness Based on Takeshima

Petitioner argues that claims 1–7 would have been obvious in view of Takeshima. Pet. 53–70. In support of its showing, Petitioner relies upon the

Leeb Declaration. *Id.* (citing Ex. 1002). We have reviewed Petitioner's assertions and supporting evidence. For the reasons discussed below, and based on the record before us, we determine that Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that at least one challenged claim would have been obvious in view of Takeshima.

Petitioner relies on Takeshima to disclose or suggest all of the recitations of independent claim 1. Pet. 53–59. Regarding limitation 1[d], Petitioner argues that Takeshima illustrates MOSFETs 8a, 8b positioned on the top and bottom surfaces, respectively, of a PCB. *Id.* at 57 (citing Ex. 1010, 8:46–47, 10:51–55, Fig. 2). Petitioner argues that it would have been obvious to an ordinarily skilled artisan "to employ the half-bridge converter taught in Takeshima's Figure 14." *Id.* (citing Ex. 1002 ¶ 63). Petitioner argues that this modification would "provid[e] additional control by using MOSFET switches instead of diodes." *Id.* at 57–58 (citing Ex. 1010, Figs. 2, 14; Ex. 1002 ¶ 163).

Regarding limitation 1[e], Petitioner argues that an ordinarily skilled artisan "would have known to operate Takeshima's half-bridge converter with balanced power cycles on the top and bottom sides in order to avoid saturating the transformer." Pet. 59 (citing Ex. 1002 ¶ 166; Ex. 1008, 152, 154, Fig. 6.18; Ex. 1010, 11:44–51; Ex. 1012, Figs. 2, 3). Petitioner argues that an ordinarily skilled artisan "would have expected [the four MOSFETs] to dissipate power at levels Pt and Pb that were equal or at least approximately equal." *Id.* (citing Ex. 1002 ¶ 167; Ex. 1015, 9:19–23).

Patent Owner contests this challenge for a number of reasons. Prelim. Resp. 51–58. First, Patent Owner argues that Petitioner has provided inadequate motivation to modify the teachings of Takeshima. *Id.* at 51–54.

Patent Owner argues "the circuit of [Takeshima] Fig. 14 *already has a layout*, and it has *no MOSFETs on the bottom of the device*"; rather, "MOSFETs 8a-8d [are] located on the *top* of the PCB." *Id.* at 52 (citing Ex. 1010, 8:8–18, Fig. 15A; Ex. 2001 ¶ 128). Patent Owner argues that "Takeshima explains with respect to another embodiment, that of Fig. 5, that Takeshima intentionally places topologically parallel MOSFETs together." *Id.* at 53 (citing Ex. 1010, 12:53–64; Ex. 2001 ¶ 130).

We agree with Patent Owner. Petitioner proposes "to employ the half-bridge converter taught in Takeshima's Figure 14." Pet. 57. As correctly noted by Patent Owner, MOSFETs 8a, 8b, 8c, 8d in the embodiment illustrated in Figure 14 are all positioned on the top surface of the PCB, as illustrated in Figure 15A. Ex. 1010, 8:8–18, Fig. 15A. Petitioner does not explain adequately why, when "employ[ing] the half-bridge converter taught in Takeshima's Figure 14," two of the MOSFETs would instead be relocated to the bottom surface of the PCB. Notably, neither Petitioner nor Dr. Leeb explains how using MOSFETs in place of diodes provides additional control. *See* Pet. 57–58; Ex. 1002 ¶ 163. Such a conclusory assertion fails to persuade us that it would have been obvious to an ordinarily skilled artisan to simply replace diodes 10a, 10b of Takeshima's first preferred embodiment with MOSFETs 8c, 8d of the third preferred embodiment as suggested by Petitioner. *See* Ex. 1010, 19:52–56 ("the switching power supply device 100 described in the first preferred embodiment and the switching power supply device described in the [third preferred] embodiment *greatly differ* in their operations" (emphasis added)). Moreover, Figure 5 illustrates "switching power supply device 200 according to the first preferred embodiment" having four MOSFETs 8a–8d

all positioned on the top surface of the PCB. *Id.* at 11:56–67, 12:39–41, Fig. 5. Notably, neither Petitioner not Dr. Leeb address the configuration of Takeshima's first preferred embodiment as illustrated in Figure 5.

Next, Patent Owner argues that the circuit illustrated in Takeshima Figure 14 "has capacitors 6a and 6b in series with transformer primary winding 9a that preclude transformer saturation and enable it to operate with a variable, unbalanced duty cycle." Prelim. Resp. 55 (citing Ex. 2001 ¶ 134). Patent Owner argues that "this arrangement prevents transformer saturation, because the voltage-dividing capacitors block DC components of the transformer current. *Id.* at 56 (citing Ex. 2001 ¶ 135; Ex. 2008, 100, Fig. 4.20B). Patent Owner concludes that Petitioner's asserted rationale that an ordinarily skilled artisan would know to operate Takeshima with balanced power cycles to avoid saturating the transformer is, therefore, incorrect. *Id.* at 57 (citing Ex. 211 ¶ 136).

We are persuaded by Patent Owner's arguments, which comport with the prior testimony of Dr. Leeb discussed above. *See* Prelim. Resp. 41–43, 56–57.

Finally, Patent Owner argues that the embodiment of Takeshima Figure 14 "is a regulating converter that uses [pulse-width modulation] to operate both primary and secondary MOSFETs with a variable duty cycle to regulate the output voltage," such that the "output MOSFETs operate with a variable duty cycle, in unbalanced fashion." Prelim. Resp. 57–58 (citing Ex. 1010, 20:10–23; Ex. 2001 ¶ 137).

We agree that Petitioner has not adequately explained why an ordinarily skilled artisan would operate Takeshima's converter with balanced power cycles. *See* Pet. 59. The Petition glosses over how

Takeshima's various circuits operate and does not address the fact that the circuits of the first preferred embodiment and the third preferred embodiment "greatly differ in their operations." *See* Ex. 1010, 19:52–56.

For at least the foregoing reasons, Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that claim 1, or its dependent claims 2–7, would have been obvious in view of Takeshima.

I. Asserted Obviousness Based on Takeshima and Spiazzi

Petitioner argues that claims 1–7 would have been obvious in view of Takeshima and Spiazzi. Pet. 70–76. In support of its showing, Petitioner relies upon the Leeb Declaration. *Id.* (citing Ex. 1002). We have reviewed Petitioner's assertions and supporting evidence. For the reasons discussed below, and based on the record before us, we determine that Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that at least one challenged claim would have been obvious in view of the combination of Takeshima and Spiazzi.

Petitioner relies on Takeshima to disclose most of the recitations of independent claim 1 as set forth above in the challenge based on Takeshima alone, and relies on Spiazzi to teach that Takeshima's circuit would operate with "equal (or at least approximately equal) power dissipation levels Pt and Pb" for the reasons discussed above regarding the challenge based on Ericsson-BMR and Spiazzi. Pet. 70–74. Petitioner argues that "when the portions of Takeshima converter relied upon in the asserted embodiment are operated in the environment of Spiazzi, the power dissipation levels Pt and Pb would indeed at least be 'similar' and well within 150% of each other." *Id.* at 72. Petitioner argues that "Spiazzi expressly recognizes that its half-

bridge converter should be powered with equal current, voltage, and power on the top and bottom MOSFET switches" as evidenced by Figure 1b. *Id.* at 72–73.

Patent Owner contests this challenge for a number of reasons. Prelim. Resp. 58–62. First, Patent Owner argues that Petitioner's challenge is deficient because Petitioner does not explain with sufficient clarity what "the combination" of Takeshima and Spiazzi entails or "what it means to 'combin[e] Takeshima with Spiazzi in Spiazzi's environment.'" Prelim. Resp. 59 (alteration in original) (quoting Pet. 74).

We agree that the Petition does not set forth the challenge with requisite particularity. *See* 35 U.S.C. § 312 (a)(3) (requiring petitions to "identif[y], in writing and with particularity, each claim challenged, the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge to each claim"); *Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) ("It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify 'with particularity' the 'evidence that supports the grounds for the challenge to each claim.'"). For example, Petitioner does not explain what "the asserted embodiment" or "operated in the environment of Spiazzi" mean. *See* Pet. 72.

Next, Patent Owner argues that the combination of Takeshima and Spiazzi suffers the same deficiencies discussed above regarding the challenge based on Takeshima alone and the challenge based on Ericsson-BMR and Spiazzi. Prelim. Resp. 60. Patent Owner argues that an ordinarily skilled artisan would not expect Takeshima to exhibit the thermal

outputs measured in Spiazzi because "Spiazzi and Takeshima are very different circuits." *Id.*

We agree with Patent Owner. Although Petitioner does not explain what it means by the "Takeshima converter relied upon in the asserted embodiment" (Pet. 72), to the extent Petitioner means the modified embodiment asserted in the challenge based on Takeshima alone, the same deficiencies discussed above apply to this challenge. We further agree that Petitioner does not explain adequately why the disparate circuits of Takeshima and Spiazzi would be expected to operate in the same manner and have the same thermal output.

Finally, Patent Owner argues "the Petition's reliance on the Kawanami reference (Ex. 1023) is misplaced" because "[i]ts structure is markedly different from that of both Spiazzi and Takeshima." Prelim. Resp. 61 (citing Ex. 1023 ¶ 2; Ex. 2001 ¶ 143).

We agree that Petitioner does not explain adequately how the disclosure of Kawanami is relevant to the combination of Takeshima and Spiazzi. *See* Pet. 74 (citing Ex. 1023 ¶¶ 51–52). Petitioner provides a parenthetical statement that appears to quote a few phrases from Kawanami, but Petitioner does not explain how any circuit disclosed by Kawanami is similar to those of Takeshima or Spiazzi, or assert why an ordinarily skilled artisan would look to the teachings of Kawanami when combining the teachings of Takeshima and Spiazzi.

For at least the foregoing reasons, Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that claim 1, or its dependent claims 2– 7, would have been obvious in view of the combination of Takeshima and Spiazzi.

J. Asserted Obviousness Based on Takeshima and Wanes

Petitioner argues that claims 1–7 would have been obvious in view of Takeshima and Wanes. Pet. 76–79. In support of its showing, Petitioner relies upon the Leeb Declaration. *Id.* (citing Ex. 1002). We have reviewed Petitioner's assertions and supporting evidence. For the reasons discussed below, and based on the record before us, we determine that Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that at least one challenged claim would have been obvious in view of the combination of Takeshima and Wanes.

Petitioner relies on Takeshima to disclose most of the recitations of independent claim 1 as set forth above in the challenge based on Takeshima alone, and purports to rely on Wanes to teach distribution of heat generation. Pet. 76–78. Petitioner argues that, "[i]n the asserted embodiment, Takeshima's module is in the environment of Wanes, thus confirming equal or at least approximately equal power dissipation and thus satisfying [limitation 1[e]]." *Id.* at 77 (citing Ex. 1011, 1999).

Patent Owner argues that "[t]he Petition provides no overview or explanation of what, if anything, is being modified in Takeshima" and provides "no explanation of what the 'asserted embodiment' might be, nor any explanation of what is meant by 'the environment of Wanes.'" Prelim. Resp. 63–64. Patent Owner notes that the Petition relies on Spiazzi rather than Wanes. *Id.* at 64.

We agree that the Petition does not set forth the challenge with requisite particularity. *See* 35 U.S.C. § 312 (a)(3). Petitioner quotes Spiazzi rather than Wanes. *See* Pet. 77–78 (quoting Ex. 1011, 1999). Thus, Petitioner does not explain how it relies on Wanes, and the Petition is

therefore deficient. To the extent Petitioner asserts another challenge based on Takeshima and Spiazzi, the challenge is deficient for the reasons provided above.

For at least the foregoing reasons, Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that claim 1, or its dependent claims 2– 7, would have been obvious in view of the combination of Takeshima and Wanes.

K. Asserted Obviousness Based on Ericsson-BMR and Takeshima

Petitioner argues that claims 1–7 would have been obvious in view of Ericsson-BMR and Takeshima. Pet. 79–82. In support of its showing, Petitioner relies upon the Leeb Declaration. *Id.* (citing Ex. 1002). We have reviewed Petitioner's assertions and supporting evidence. For the reasons discussed below, and based on the record before us, we determine that Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that at least one challenged claim would have been obvious in view of the combination of Ericsson-BMR and Takeshima.

Petitioner relies on Ericsson-BMR to disclose most of the recitations of independent claim 1 as set forth in the challenge based on Ericsson-BMR alone, and relies on Takeshima to teach transformer windings formed in the layers of a PCB. Pet. 79–81. Petitioner argues that "[Ericsson-BMR's] output FETs could have been those that are placed symmetrically" and symmetrical placement would have been an obvious design choice. *Id.* at 81.

Petitioner's reliance on Takeshima fails to overcome the deficiencies noted above regarding Petitioner's challenge based on Ericsson-BMR alone.

See Prelim. Resp. 65. Therefore, Petitioner's challenge is unpersuasive for the same reasons discussed above.

Furthermore, Petitioner's conclusory assertion fails to explain adequately how the positioning of MOSFETs on a PCB is a mere design choice, as Petitioner does not address the requirements for design choice. *See* Prelim. Resp. 65; *see also In re Kuhle*, 526 F.2d 553, 555 (CCPA 1975) (finding that the use of the claimed feature "would be an obvious matter of design choice" when it "solves no stated problem" and "presents no novel or unexpected result" over the disclosed alternatives); *Ex parte Maeda*, Appeal No. 2010-009814, at 6–7 (PTAB Oct. 23, 2012) (designated informative) ("'design choice' may be appropriate where the applicant fails to set forth any reasons why the differences between the claimed invention and the prior art would result in a different function or give unexpected results" (citing *In re Chu*, 66 F.3d 292, 298–99 (Fed. Cir. 1995)). Additionally, Petitioner's assertion that the MOSFETs of Ericsson-BMR "*could* have been . . . placed symmetrically" (Pet. 81 (emphasis added)) fails to explain why the MOSFETs *would* have been so positioned. *See In re Etter*, 756 F.2d 852, 859 (Fed. Cir. 1985) (en banc) (explaining that the obviousness inquiry does not ask "whether the references could be physically combined but whether the claimed inventions are rendered obvious by the teachings of the prior art as a whole").

For at least the foregoing reasons, Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that claim 1, or its dependent claims 2– 7, would have been obvious in view of the combination of Ericsson-BMR and Takeshima.

L. Asserted Obviousness Based on Spiazzi and Wanes

Petitioner argues that claims 1–7 would have been obvious in view of Spiazzi and Wanes. Pet. 83–94. In support of its showing, Petitioner relies upon the Leeb Declaration. *Id.* (citing Ex. 1002). We have reviewed Petitioner's assertions and supporting evidence. For the reasons discussed below, and based on the record before us, we determine that Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that at least one challenged claim would have been obvious in view of the combination of Spiazzi and Wanes.

Petitioner relies on Spiazzi to disclose most of the recitations of independent claim 1, and relies on Wanes to teach transformer windings formed in the layers of a PCB. Pet. 83–91. Regarding limitation 1[d], Petitioner argues that "Spiazzi's Figure 5 shows a set of four MOSFETs labelled Q_1 that are mounted on the top surface of the PCB and are overlapping with a set of four MOSFETs labelled Q_2 mounted on the bottom surface of the PCB." *Id.* at 87. Petitioner maps the Q_1 MOSFETs to the recited first set and the Q_2 MOSFETs to the recited second set. *Id.* at 88–89 (citing Ex. 1002 ¶ 251).

Regarding limitation 1[e], Petitioner argues that Spiazzi discloses similar thermal mapping results for its top and bottom PCB surfaces, and an ordinarily skilled artisan "would therefore have recognized that, in Spiazzi, the power dissipation levels Pt and Pb would at least be 'similar' and well within 150% of each other on top and bottom." Pet. 89 (citing Ex. 1011, 1999–2000; Ex. 1002 ¶ 253). Petitioner argues that an ordinarily skilled artisan "would have expected this result in Spiazzi's physical environment and configuration because Spiazzi expressly recognizes that its half-bridge

converter should be powered with equal current, voltage, and power on the top and bottom MOSFETs." *Id.* (footnote omitted).

Citing its arguments presented for the challenge based on Ericsson-BMR and Spiazzi, Patent Owner argues that "Spiazzi's input MOSFETs are entirely located on the top side of the device, and Spiazzi's own measurements indicate that MOSFETs on the top side would dissipate 3.31 times the power of MOSFETs on the bottom side." Prelim. Resp. 68 (citing Ex. 1011, 4; Ex. 2001 ¶ 160). Continuing, Patent Owner argues that "[t]he Petition's citation to Huber (Ex. 1012) is taken out of context." *Id.* (citing Ex. 2001 ¶ 160); *see also* Pet. 90–91 (quoting Ex. 1012, 82).

We are persuaded that Petitioner's analysis of Spiazzi's teachings is, at best, incomplete for the reasons set forth above regarding the challenge based on Ericsson-BMR and Spiazzi. Petitioner again fails to consider the presence and effects of the primary MOSFETs HB_1, HB_2, which are only on the top side of the PCB with no corresponding components on the bottom side.

We also agree that Petitioner does not explain adequately how the disclosure of Huber is relevant to the combination of Spiazzi and Wanes. *See* Pet. 90–91 (citing Ex. 1012, 82). Petitioner provides a purported quotation from Huber, but Petitioner does not explain how any circuit disclosed by Huber is similar to those of Spiazzi and Wanes, or assert why an ordinarily skilled artisan would look to the teachings of Huber when combining the teachings of Spiazzi and Wanes.

For at least the foregoing reasons, Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that claim 1, or its dependent

claims 2– 7, would have been obvious in view of the combination of Spiazzi and Wanes.

M. Asserted Obviousness Based on BMR-2008 Alone or in Combination with Spiazzi, Wanes, or Takeshima

Petitioner argues that claims 1–5 and 7 would have been obvious in view of BMR-2008 (Pet. 34), claims 1–5 and 7 would have been obvious in view of BMR-2008 and Spiazzi (*id.* at 39–40), claims 1–7 would have been obvious in view of BMR-2008 and Wanes (*id.* at 53), and claims 1–7 would have been obvious in view of BMR-2008 and Takeshima (*id.* at 82–83). Regarding the challenge based on BMR-2008 alone, Petitioner argues that "[t]he relevant teachings of BMR-2008 are substantially the same as the relevant teachings of Ericsson-BMR, including the symmetry and fundamental circuit diagram of a full-bridge converter." *Id.* at 34. Petitioner concludes that, "[a]s a result, [c]laims 1-5 and 7 are rendered obvious by BMR-2008 for the same reasons as they are rendered obvious by Ericsson-BMR." *Id.* (citing Ex. 1002 ¶¶ 102–103). Petitioner makes substantially similar arguments regarding the other challenges based on BMR-2008. *See id.* at 39–40, 53, 82–83).

Petitioner fails to identify with requisite particularity how BMR-2008 renders the challenged claims obvious. *See* 35 U.S.C. § 312 (a)(3). Petitioner has made no showing of the grounds on which the challenged claims are based; Petitioner makes no mapping whatsoever of the BMR-2008 disclosure to the challenged claims, instead suggesting that we compare the disclosures of BMR-2008 and Ericsson-BMR. This is insufficient to meet Petitioner's obligation to identify with particularity how the asserted references satisfy the requirements of the challenged claims.

For at least the foregoing reasons, Petitioner does not demonstrate a reasonable likelihood of prevailing in showing that claim 1, or its dependent claims 2–7, would have been obvious in view of Ericsson-BMR alone or in combination with Spiazzi, Wanes, or Takeshima.

III. PATENT OWNER'S MOTION TO SEAL

In connection with the Preliminary Response, Patent Owner filed an Unopposed Motion to Seal. Paper 10 ("Motion"). Patent Owner seeks to seal Exhibit 2032 and portions of the Preliminary Response and Exhibit 2001. *Id.* at 1.

A. Motion to Seal

There is a strong public policy in favor of making information filed in an *inter partes* review open to the public, especially because the proceeding determines the patentability of claims in an issued patent and, therefore, affects the rights of the public. Under 35 U.S.C. § 316(a)(1) and 37 C.F.R. § 42.14, the default rule is that all papers filed in an *inter partes* review are open and available for access by the public; a party, however, may file a concurrent motion to seal and the information at issue is sealed pending the outcome of the motion. It is only "confidential information" that is protected from disclosure. 35 U.S.C. § 316(a)(7). In that regard, the Consolidated Trial Practice Guide[7] ("CTPG") provides guidance:

> The rules aim to strike a balance between the public's interest in maintaining a complete and understandable file history and the parties' interest in protecting truly sensitive information.
> . . . .

[7] *Available at* https://www.uspto.gov/TrialPracticeGuideConsolidated.

> 2. Confidential information: The rules identify confidential information in a manner consistent with Federal Rule of Civil Procedure 26(c)(1)(G), which provides for protective orders for trade secret or other confidential research, development, or commercial information. 37 C.F.R. § 42.54.

CTPG 19.

The standard for granting a motion to seal is "for good cause." 37 C.F.R. § 42.54(a). The filing party bears the burden of proof in showing entitlement to the relief requested in a motion to seal. *Id.* § 42.20(c). To show good cause to seal, the movant: must provide a sufficient explanation as to why the information sought to be sealed is confidential; must demonstrate that the information is not excessively redacted; and must demonstrate that, on balance, the strong public policy in maintaining a complete and understandable record is outweighed by harm that would be caused to the movant by disclosure of the information and the need of either party to rely specifically on the information. *Argentum Pharm. LLC v. Alcon Research, Ltd.*, IPR2017-01053, Paper 27 at 3–4 (PTAB Jan. 19, 2018) (designated informative).

1. Exhibit 2032

Patent Owner seeks to seal Exhibit 2032 in its entirety. Motion 1. Patent Owner asserts that "Exhibit 2032 includes highly-sensitive information regarding the structure and operation of certain [Patent Owner] products," including "highly-sensitive details regarding the design of [Patent Owner's] products, including circuit diagrams," and that the information "is not publicly available." *Id.* at 3. Patent Owner asserts that Exhibit 2032 is cited in the declaration of Patrizio Vinciarelli (Ex. 2030), which makes

"clear that Exhibit 2032 is intended to show that [Patent Owner] NBM2317 products meet certain claims of the" '761 patent. *Id.*

Patent Owner asserts that it will face "concrete harm" if the information contained in Exhibit 2032 becomes publicly available because "[c]ompetitors and other third-parties could exploit the information for their own benefit to design competitive products, thereby saving time and research effort." Motion 3.

We have reviewed Exhibit 2032 and are persuaded that it contains information that is confidential and, therefore, that good cause exists to maintain this exhibit under seal. We note that this exhibit is not cited or relied upon in this Decision. Accordingly, Patent Owner's motion to seal Exhibit 2032 is *granted*.

2. Preliminary Response and Exhibit 2001

Patent Owner seeks to seal portions of the Preliminary Response and Exhibit 2001. Motion 1. Patent Owner asserts that "[t]he Preliminary Response and Ex. 2001 contain a brief discussion of Exhibit 1025" and notes that "Exhibit 1025 was filed under seal by the Petitioner, and was the subject of a motion to seal (Paper 3)." *Id.* at 4. Therefore, Patent Owner "moves to seal the portions of the Preliminary Response and Ex. 2001 that discuss Ex. 1025." *Id.* Patent Owner notes that it filed redacted, publicly-available copies of the Preliminary Response and Exhibit 2001 "to remove details contained within Ex. 1025." *Id.*

Exhibit 1025 was sealed in Paper 8. We have reviewed the redacted portions of the Preliminary Response and Exhibit 2001 and agree that the redactions are minor and limited to discussion of the contents of

Exhibit 1025. Patent Owner filed redacted versions of these documents. We note that we do not rely on the redacted information in making our conclusions in this proceeding. Accordingly, Patent Owner's motion to seal portions of the Preliminary Response and Exhibit 2001 is *granted*.

3. Public Availability of Sealed Documents

As a reminder, confidential information that is subject to a protective order ordinarily becomes public forty-five days after final judgment in a trial. CTPG 21–22. However, after denial of a petition to institute a trial or after final judgment in a trial, a party may file a motion to expunge confidential information from the record prior to the information becoming public in accordance with 37 C.F.R. § 42.56.

B. Protective Order

The Board encourages the parties to adopt the Board's default protective order if they conclude that a protective order is necessary. *See* CTPG 107–22 (App. B, Protective Order Guidelines and Default Protective Order). Parties wishing to enter a protective order other than the default protective order must file a copy of the proposed protective order. *Id.* at 113–14. Although a scheduling order has not been entered in this proceeding, the Board's scheduling orders routinely instruct parties who choose to propose a protective order deviating from the default protective order to file a marked-up comparison of the proposed and default protective orders showing the differences between the two and explain why good cause exists to deviate from the default protective order.

The Board's default protective Order has been entered in this proceeding. Paper 8, 4. Nonetheless, Patent Owner purports to "request[]

that the Board enter the Stipulated Protective Order attached as Appendix A." Motion 4. Patent Owner also purports to file a "redline version showing changes to the Default Protective Order" as Appendix B. *Id.* at 5. However, Patent Owner did not submit a copy of any "Stipulated Protective Order" or a "redline version" thereof, and the Motion does not include Appendixes A or B. We note that Patent Owner filed both its proposed protective order and a marked-up comparison vis-à-vis the default protective order in two other proceedings between the parties. *See* IPR2024-00187, Paper 8; IRP2024-00134, Paper 7.

According, Patent Owner's request to enter a "Stipulated Protective Order" is *denied*. Instead, "this matter shall be governed by the Default Protective Order." Paper 8, 4.

We note that Exhibit 2032 contains indications other than the "PROTECTIVE ORDER MATERIAL" designation set forth in the default protective order and Paper 8. In this proceeding, we assign no heightened level of confidentiality to Exhibit 2032; instead, Exhibit 2032 is to be treated in accordance with the Board's default protective order.

IV. CONCLUSION

For the foregoing reasons, we are not persuaded that the Petition establishes a reasonable likelihood that Petitioner would prevail in any of its challenges to claims 1–7 of the '761 patent.

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is *denied*, and no trial is instituted; and

FURTHER ORDERED that Patent Owner's Motion to Seal (Paper 10) is *granted in part* such that the Preliminary Response, Exhibit 2001, and Exhibit 2032 are sealed, and *denied in part* such that the asserted Stipulated Protective Order is not entered.

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